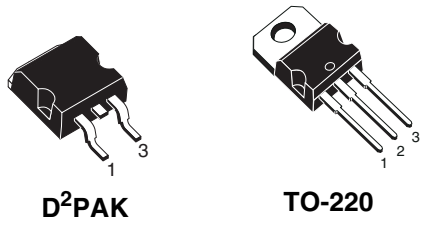
# STB80PF55
# STP80PF55

P-channel 55 V, 0.016 Ω, 80 A TO-220, $D^2PAK$
STripFET™ II Power MOSFET

## Features

| Type | $V_{DSS}$ | $R_{DS(on)}$ | $I_D$ |
|---|---|---|---|
| STP80PF55 | 55V | <0.018Ω | 80A |
| STB80PF55 | 55V | <0.018Ω | 80A |

- Extremely dv/dt capability
- 100% avalanche tested
- Application oriented characterization




## Application

- Switching applications

## Description

These Power MOSFETs are the latest development of STMicroelectronics unique "single feature size" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps allowing remarkable manufacturing reproducibility.

**Figure 1. Internal schematic diagram**

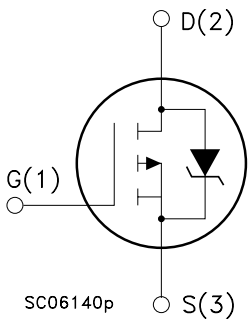



**Table 1. Device summary**

| Order code | Marking | Package | Packaging |
|---|---|---|---|
| STP80PF55 | P80PF55 | TO-220 | Tube |
| STB80PF55 | B80PF55 | $D^2PAK$ | Tape and reel |

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DS}$ | Drain-source voltage ($V_{GS}$ = 0) | 55 | V |
| $V_{GS}$ | Gate-source voltage | ±16 | V |
| $I_D$ (1) | Drain current (continuous) at $T_C$ = 25°C | 80 | A |
| $I_D$ | Drain current (continuous) at $T_C$ = 100°C | 57 | A |
| $I_{DM}$ (2) | Drain current (pulsed) | 320 | A |
| $P_{TOT}$ | Total dissipation at $T_C$ = 25°C | 300 | W |
| | Derating factor | 2 | W/°C |
| dv/dt (3) | Peak diode recovery voltage slope | 7 | V/ns |
| $E_{AS}$ (4) | Single pulse avalanche energy | 1.4 | J |
| $T_j$<br>$T_{stg}$ | Operating junction temperature<br>Storage temperature | -55 to 175 | °C |

1. Current limited by package.
2. Pulse width limited by safe operating area .
3. $I_{SD} \leq 40A$, di/dt $\leq$ 300 A/µs, $V_{DD}$=80% $V_{(BR)DSS}$.
4. Starting Tj=25°C, $I_D$=80A, $V_{DD}$=40V.

**Table 3. Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{thj-case}$ | Thermal resistance junction-case max | 0.5 | °C/W |
| $R_{thj-a}$ | Thermal resistance junction-ambient max | 62.5 | °C/W |
| $T_l$ | Maximum lead temperature for soldering purpose | 300 | °C |

*Note: For the P-CHANNEL MOSFET actual polarity of voltages and current has to be reversed*

# 2 Electrical characteristics

($T_{CASE}$=25°C unless otherwise specified)

**Table 4. On/off states**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $I_D$ = 250 mA, $V_{GS}$ = 0 | 55 | | | V |
| $I_{DSS}$ | Zero gate voltage drain current ($V_{GS}$ = 0) | $V_{DS}$ = Max rating<br>$V_{DS}$ = Max rating, $T_C$=125 °C | | | 1<br>10 | µA<br>µA |
| $I_{GSS}$ | Gate-body leakage current ($V_{DS}$ = 0) | $V_{GS}$ = ±16 V | | | ±10 | µA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 2 | 3 | 4 | V |
| $R_{DS(on)}$ | Static drain-source on resistance | $V_{GS}$ = 10 V, $I_D$ = 40 A | | 0.016 | 0.018 | Ω |

**Table 5. Dynamic**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $g_{fs}$ | Forward transconductance | $V_{DS}$ > $I_{D(on)}$ x $R_{DS(on)max}$, $I_D$= 40 A | - | 32 | | S |
| $C_{iss}$<br>$C_{oss}$<br>$C_{rss}$ | Input capacitance<br>Output capacitance<br>Reverse transfer capacitance | $V_{DS}$ = 25 V, f = 1MHz, $V_{GS}$ = 0 | - | 5500<br>1130<br>600 | | pF<br>pF<br>pF |
| $Q_g$<br>$Q_{gs}$<br>$Q_{gd}$ | Total gate charge<br>Gate-source charge<br>Gate-drain charge | $I_D$ = 25 A, $V_{DD}$ = 80 V, $V_{GS}$ = 10 V | - | 190<br>27<br>65 | 258 | nC<br>nC<br>nC |

**Table 6. Switching times**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$<br>$t_r$ | Turn-on delay time<br>Rise time | $V_{DD}$=25 V, $I_D$=40 A, $R_G$=4.7 Ω, $V_{GS}$=10 V | - | 35<br>190 | - | ns<br>ns |
| $t_{d(off)}$<br>$t_f$ | Turn-off delay time<br>Fall time | $V_{DD}$=25 V, $I_D$=40 A, $R_G$=4.7 Ω, $V_{GS}$=10 V | - | 165<br>80 | - | ns<br>ns |
| $t_{r(Voff)}$<br>$t_f$<br>$t_c$ | Off-voltage rise time<br>Fall time<br>Cross-over time | $V_{clamp}$=40 V, $I_D$=80 A, $R_G$=4.7 Ω, $V_{GS}$=10 V | - | 60<br>40<br>85 | - | ns<br>ns<br>ns |

**Table 7. Source drain diode**

| Symbol | Parameter | Test condictions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$<br>$I_{SDM}$ (1) | Source-drain current<br>Source-drain current (pulsed) | | - | | 10<br>40 | A<br>A |
| $V_{SD}$ (2) | Forward on voltage | $I_{SD}$ = 80 A, $V_{GS}$ = 0 | - | | 1.6 | V |
| $t_{rr}$<br>$Q_{rr}$<br>$I_{RRM}$ | Reverse recovery time<br>Reverse recovery charge<br>Reverse recovery current | $I_{SD}$ = 80 A, di/dt = 100 A/µs<br>$V_{DD}$ = 25 V, $T_j$ =150 °C | - | 110<br>495<br>9 | | ns<br>µC<br>A |

1. Pulse width limited by Tjmax .
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5 %.

*Note: For the P-CHANNEL MOSFET actual polarity of voltages and current has to be reversed*

## 2.1 Electrical characteristics (curves)

**Figure 2. Safe operating area for TO-220 and D²PAK**

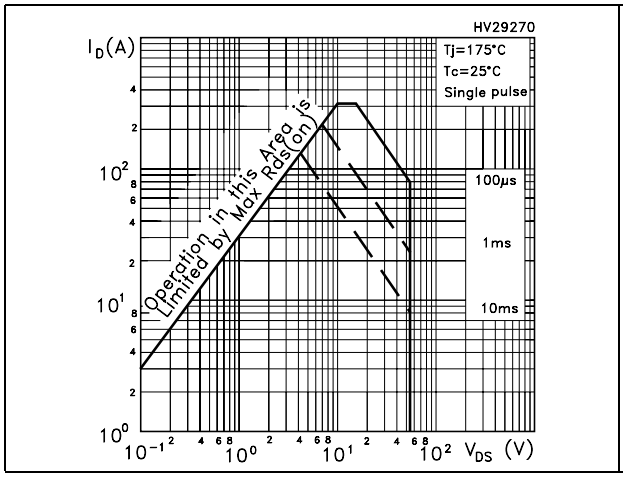



**Figure 3. Thermal impedance for TO-220 and D²PAK**

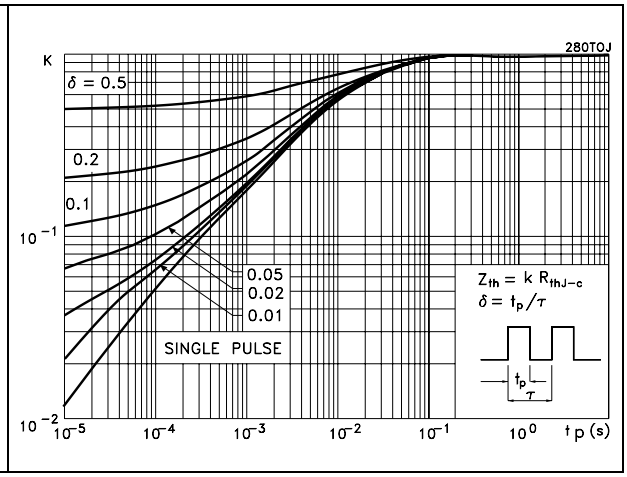



**Figure 4. Output characterisics**

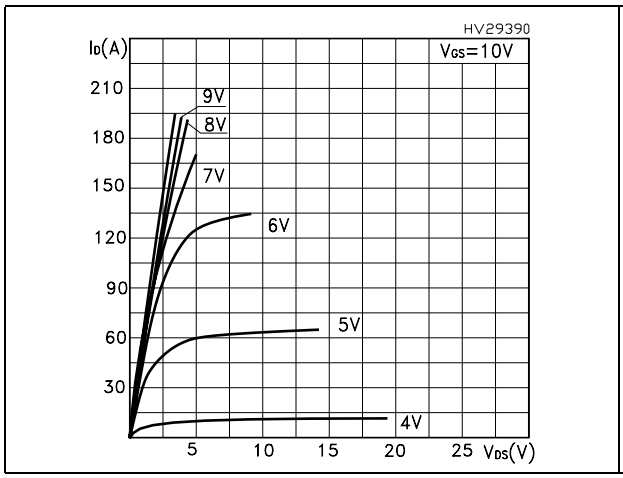



**Figure 5. Transfer characteristics**

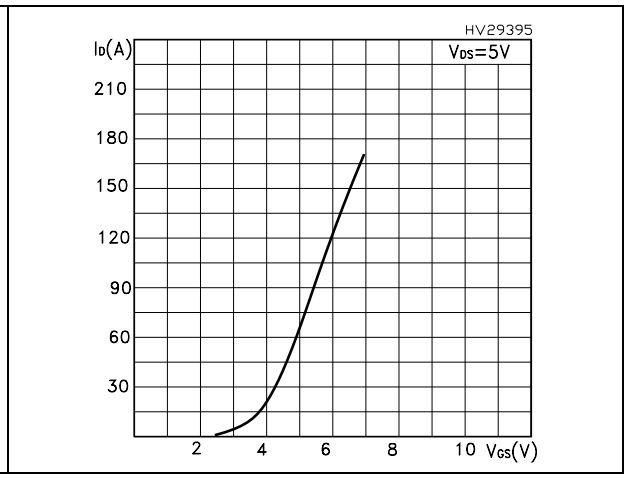



**Figure 6. Transconductance**

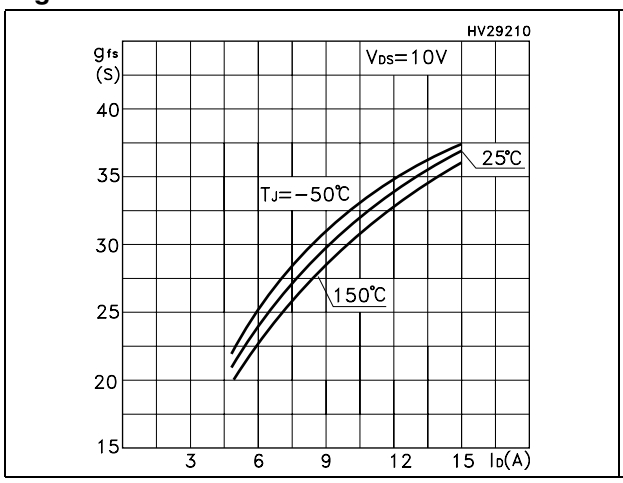



**Figure 7. Static drain-source on resistance**