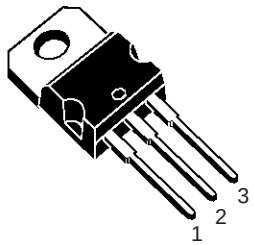
STP80NS04Z

N - CHANNEL CLAMPED 7.5mΩ - 80A - TO-220
FULLY PROTECTED MESH OVERLAY™ MOSFET

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STP80NS04Z	CLAMPED	<0.008 Ω	80 A

- TYPICAL $R_{DS(on)}$ = 0.0075 Ω
- 100% AVALANCHE TESTED
- LOW CAPACITANCE AND GATE CHARGE
- 175 °C MAXIMUM JUNCTION TEMPERATURE

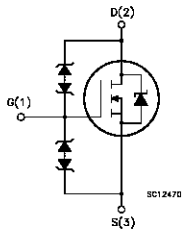


TO-220

DESCRIPTION

This fully clamped Mosfet is produced by using the latest advanced Company's Mesh Overlay process which is based on a novel strip layout.
The inherent benefits of the new technology coupled with the extra clamping capabilities make this product particularly suitable for the harshest operation conditions such as those encountered in the automotive environment. Any other application requiring extra ruggedness is also recommended.

INTERNAL SCHEMATIC DIAGRAM



APPLICATIONS

- ABS, SOLENOID DRIVERS
- MOTOR CONTROL
- DC-DC CONVERTERS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	CLAMPED	V
V_{DG}	Drain- gate Voltage	CLAMPED	V
V_{GS}	Gate-source Voltage	CLAMPED	V
I_D	Drain Current (continuous) at T_c = 25 °C	80	A
I_D	Drain Current (continuous) at T_c = 100 °C	60	A
I_{DG}	Drain Gate Current (continuous)	± 50	mA
I_{GS}	Gate Source Current (continuous)	± 50	mA
I_{DM}(•)	Drain Current (pulsed)	320	A
P_{tot}	Total Dissipation at T_c = 25 °C	160	W
	Derating Factor	1.06	W/°C
V_{ESD}(G-S)	Gate-Source ESD (HBM - C= 100pF, R=1.5 kΩ)	2	kV
V_{ESD}(G-D)	Gate-Drain ESD (HBM - C= 100pF, R=1.5 kΩ)	4	kV
V_{ESD}(D-S)	Drain-Source ESD (HBM - C= 100pF, R=1.5 kΩ)	4	kV
T_{stg}	Storage Temperature	-65 to 175	°C
T_j	Max. Operating Junction Temperature	-40 to 175	°C

(•) Pulse width limited by safe operating area

(1) $I_{SD} \leq 80$ A, di/dt ≤ 300 A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$

THERMAL DATA

$R_{thj-case}$	Thermal Resistance Junction-case	Max	0.94	$^oC/W$
$R_{thj-case}$	Thermal Resistance Junction-case	Typ	0.65	$^oC/W$
$R_{thj-amb}$	Thermal Resistance Junction-ambient	Max	62.5	$^oC/W$
$R_{thc-sink}$	Thermal Resistance Case-sink	Typ	0.5	$^oC/W$
T_l	Maximum Lead Temperature For Soldering Purpose		300	^oC

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max, $\delta < 1\%$)	80	A
E_{AS}	Single Pulse Avalanche Energy (starting $T_j = 25\ ^oC$, $I_D = I_{AR}$, $V_{DD} = 30$ V)	500	mJ

ELECTRICAL CHARACTERISTICS ($T_{case} = 25\ ^oC$ unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CLAMP}	Drain-Gate Breakdown Voltage	$I_D = 1$ mA $V_{GS} = 0$ $-40 < T_j < 175\ ^oC$	33			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = 16$ V $T_j = 175\ ^oC$			50	µA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 10$ V $T_j = 175\ ^oC$ $V_{GS} = \pm 16$ V $T_j = 175\ ^oC$			50 150	µA µA
V_{GSS}	Gate-Source Breakdown Voltage	$I_G = 100$ µA	18			V

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$ $I_D = 1$ mA $-40 < T_j < 150\ ^oC$	1.7	3	4.2	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10$V $I_D = 40$ A $V_{GS} = 16$V $I_D = 40$ A		8 7.5	9 8	mΩ mΩ
$I_{D(on)}$	On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $V_{GS} = 10$ V	80			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (*)	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $I_D = 40$ A	30	50		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25$ V f = 1 MHz $V_{GS} = 0$		4000 1250 230	5400 1700 320	pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD} = 16 V I_D = 80 A V_{GS} = 10 V		105 24 41	142	nC nC nC

SWITCHING OFF

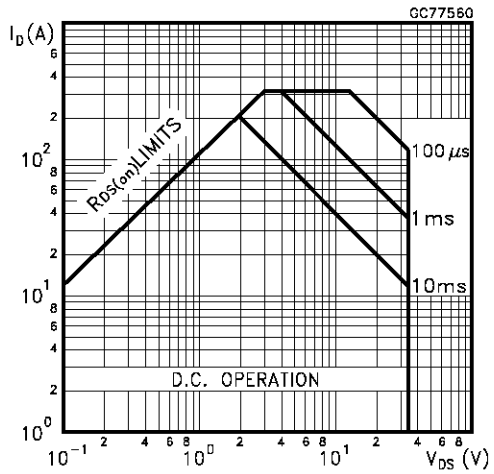
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	V_{CLAMP} = 30 V I_D = 80 A R_G =4.7 Ω V_{GS} = 10 V (see test circuit, figure 5)		60 140 220	80 190 300	ns ns ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (•)	Source-drain Current Source-drain Current (pulsed)				80 320	A A
V_{SD} (∗)	Forward On Voltage	I_{SD} = 80 A V_{GS} = 0			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 80 A di/dt = 100 A/µs V_r = 25 V T_j = 150 °C (see test circuit, figure 5)		75 0.21 6		ns µC A

(∗) Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %
(•) Pulse width limited by safe operating area

Safe Operating Area



Thermal Impedance