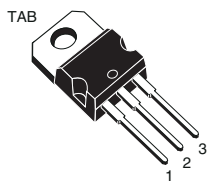
STP80N6F6

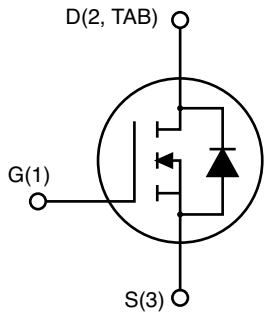
Automotive-grade N-channel 60 V, 4.4 mΩ typ., 80 A STripFET™ VI DeepGATE™ Power MOSFET in a TO-220 package

Datasheet - production data



TO-220

Figure 1. Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STP80N6F6	60 V	5 mΩ	80 A(1)

1. Current limited by package

- Designed for automotive applications and AEC-Q101 qualified
- Low gate charge
- Very low on-resistance
- High avalanche ruggedness

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the 6th generation of STripFET™ DeepGATE™ technology, with a new gate structure. The resulting Power MOSFET exhibits the lowest $R_{DS(on)}$ in all packages.

Table 1. Device summary

Order code	Marking	Packages	Packaging
STP80N6F6	80N6F6	TO-220	Tube

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	60	V
V_{GS}	Gate-source voltage	± 20	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	80	A
I_D (1)	Drain current (continuous) at T_C = 100 °C	80	A
I_{DM} (1)	Drain current (pulsed)	320	A
P_{TOT}	Total dissipation at T_C = 25 °C	120	W
	Derating factor	0.8	W/°C
T_{stg}	Storage temperature	- 55 to 175	°C
T_j	Operating junction temperature		

1. Current limited by package

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	1.25	°C/W
$R_{thj\text{-}a}$	Thermal resistance junction-ambient max	62.5	°C/W

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage (V_{GS} = 0)	I_D = 250 μA	60			V
I_{DSS}	Zero gate voltage Drain current (V_{GS} = 0)	V_{DS} = 60 V			1	μA
		V_{DS} = 60 V, T_C=125 °C			100	μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 μA	3		4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 40 A		4.4	5	mΩ

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0	-	8325	-	pF
C_{oss}	Output capacitance		-	500	-	pF
C_{rss}	Reverse transfer capacitance		-	400	-	pF
Q_g	Total gate charge	V_{DD} = 30 V, I_D = 80 A, V_{GS} = 10 V	-	147	-	nC
Q_{gs}	Gate-source charge		-	44	-	nC
Q_{gd}	Gate-drain charge		-	46	-	nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 30 V, I_D = 40 A R_G = 4.7 Ω V_{GS} = 10 V	-	40	-	ns
t_r	Rise time			71		ns
$t_{d(off)}$	Turn-off-delay time		-	132	-	ns
t_f	Fall time		-	40	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current		-		80	A
I_{SDM} (1)	Source-drain current (pulsed)		-		320	A
V_{SD} (2)	Forward on voltage	I_{SD} = 80 A, V_{GS} = 0	-		1.3	V
t_{rr}	Reverse recovery time	I_{SD} = 80 A, V_{DD} = 48 V di/dt = 100 A/μs, T_j = 150 °C	-	46		ns
Q_{rr}	Reverse recovery charge		-	65		nC
I_{RRM}	Reverse recovery current		-	2.8		A

1. Current limited by package.
2. Pulsed: pulse duration = 300 μs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

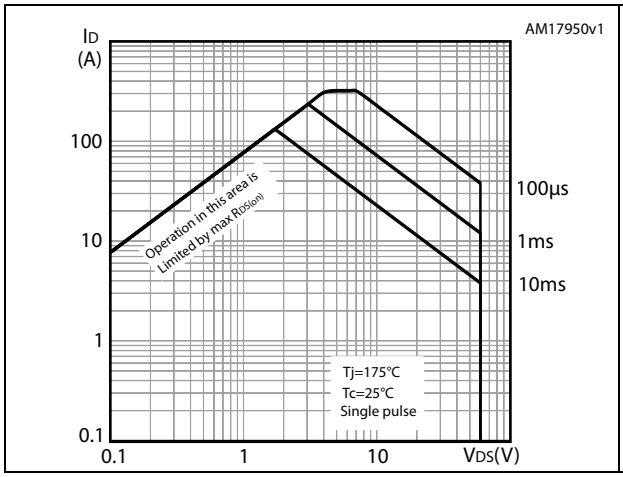


Figure 3. Thermal impedance

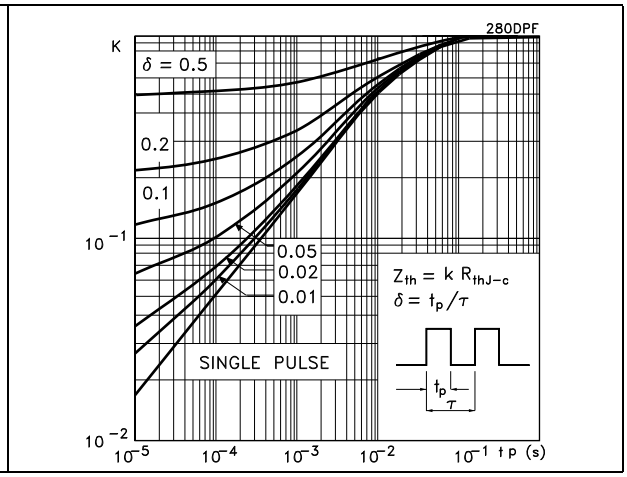


Figure 4. Output characteristics

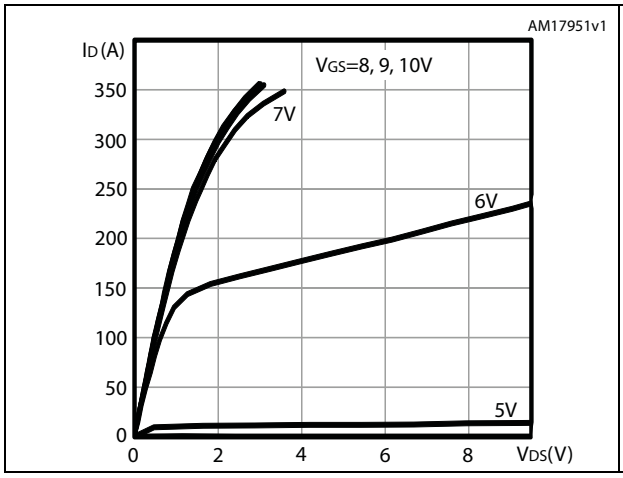


Figure 5. Transfer characteristics

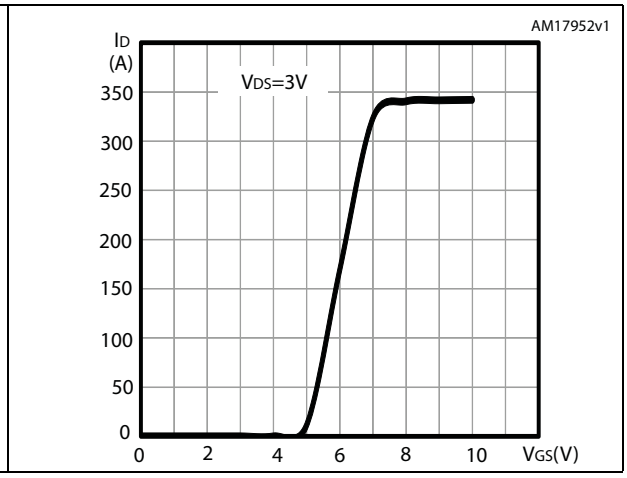


Figure 6. Gate charge vs gate-source voltage

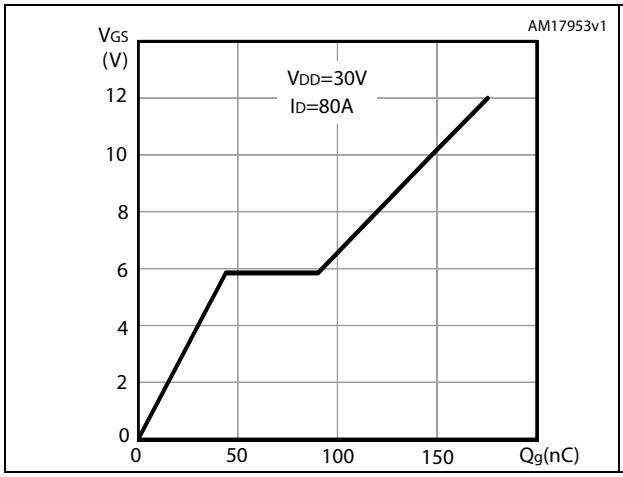


Figure 7. Static drain-source on-resistance