

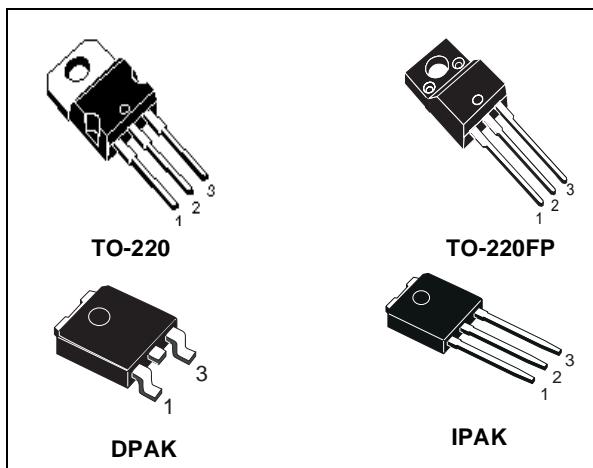
# **STP7NK40Z - STP7NK40ZFP**

## **STD7NK40Z - STD7NK40Z-1**

**N-CHANNEL 400V-0.85Ω-5.4A TO-220/TO-220FP/DPAK/IPAK**  
**Zener-Protected SuperMESH™ Power MOSFET**

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>	P <sub>w</sub>
STP7NK40Z	400 V	< 1 Ω	5.4 A	70 W
STP7NK40ZFP	400 V	< 1 Ω	5.4 A	25 W
STD7NK40Z	400 V	< 1 Ω	5.4 A	70 W
STD7NK40Z-1	400 V	< 1 Ω	5.4 A	70 W

- TYPICAL R<sub>DS(on)</sub> = 0.85 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- GATE CHARGE MINIMIZED
- VERY LOW INTRINSIC CAPACITANCES
- VERY GOOD MANUFACTURING REPEATABILITY



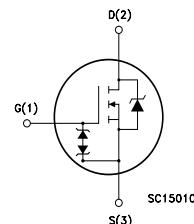
### **DESCRIPTION**

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

### **APPLICATIONS**

- HIGH CURRENT, HIGH SPEED SWITCHING
- IDEAL FOR OFF-LINE POWER SUPPLIES, ADAPTORS AND PFC
- LIGHTING

### **INTERNAL SCHEMATIC DIAGRAM**



### **ORDERING INFORMATION**

SALES TYPE	MARKING	PACKAGE	PACKAGING
STP7NK40Z	P7NK40Z	TO-220	TUBE
STP7NK40ZFP	P7NK40ZFP	TO-220FP	TUBE
STD7NK40ZT4	D7NK40Z	DPAK	TAPE & REEL
STD7NK40Z-1	D7NK40Z	IPAK	TUBE

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### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value			Unit
		STP7NK40Z	STP7NK40ZFP	STD7NK40Z STD7NK40Z-1	
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	400			V
V <sub>DGR</sub>	Drain-gate Voltage (R <sub>GS</sub> = 20 kΩ)	400			V
V <sub>GS</sub>	Gate- source Voltage	± 30			V
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 25°C	5.4	5.4 (*)	5.4	A
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 100°C	3.4	3.4 (*)	3.4	A
I <sub>DM</sub> (•)	Drain Current (pulsed)	21.6	21.6 (*)	21.6	A
P <sub>TOT</sub>	Total Dissipation at T <sub>C</sub> = 25°C	70	25	70	W
	Derating Factor	0.56	0.2	0.56	W/°C
V <sub>ESD(G-S)</sub>	Gate source ESD(HBM-C=100pF, R=1.5KΩ)	3000			V
dv/dt (1)	Peak Diode Recovery voltage slope	4.5			V/ns
V <sub>ISO</sub>	Insulation Withstand Voltage (DC)	-	2500	-	V
T <sub>j</sub> T <sub>stg</sub>	Operating Junction Temperature Storage Temperature		-55 to 150 -55 to 150		°C °C

(•) Pulse width limited by safe operating area

(1) I<sub>SD</sub> ≤ 5.4A, di/dt ≤ 200A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>j</sub> ≤ T<sub>JMAX</sub>.

(\*) Limited only by maximum temperature allowed

### THERMAL DATA

		TO-220	TO-220FP	DPAK IPAK	
R <sub>thj-case</sub>	Thermal Resistance Junction-case Max	1.78	5	1.78	°C/W
R <sub>thj-amb</sub>	Thermal Resistance Junction-ambient Max	62.5		100	°C/W
T <sub>I</sub>	Maximum Lead Temperature For Soldering Purpose	300			°C

### AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I <sub>AR</sub>	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T <sub>j</sub> max)	5.4	A
E <sub>AS</sub>	Single Pulse Avalanche Energy (starting T <sub>j</sub> = 25 °C, I <sub>D</sub> = I <sub>AR</sub> , V <sub>DD</sub> = 50 V)	130	mJ

### GATE-SOURCE ZENER DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV <sub>GSO</sub>	Gate-Source Breakdown Voltage	I <sub>GS</sub> =± 1mA (Open Drain)	30			V

### PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

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### ELECTRICAL CHARACTERISTICS ( $T_{CASE} = 25^\circ\text{C}$ UNLESS OTHERWISE SPECIFIED) ON/OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 1 \text{ mA}, V_{GS} = 0$	400			V
$I_{DSS}$	Zero Gate Voltage Drain Current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}, T_C = 125^\circ\text{C}$			1 50	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body Leakage Current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20\text{V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 50\mu\text{A}$	3	3.75	4.5	V
$R_{DS(\text{on})}$	Static Drain-source On Resistance	$V_{GS} = 10\text{V}, I_D = 2.7 \text{ A}$		0.85	1	$\Omega$

### DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs}(1)$	Forward Transconductance	$V_{DS} = 15 \text{ V}, I_D = 2.7 \text{ A}$		3.5		S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25\text{V}, f = 1 \text{ MHz}, V_{GS} = 0$		535 82 18		pF pF pF
$C_{oss \text{ eq. } (3)}$	Equivalent Output Capacitance	$V_{GS} = 0\text{V}, V_{DS} = 0\text{V} \text{ to } 400\text{V}$		53		pF

### SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on Delay Time Rise Time	$V_{DD} = 200 \text{ V}, I_D = 2.7 \text{ A}$ $R_G = 4.7\Omega, V_{GS} = 10 \text{ V}$ (Resistive Load see, Figure 3)		15 15		ns ns
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 320\text{V}, I_D = 5.4 \text{ A},$ $V_{GS} = 10\text{V}$		19 4 10	26	nC nC nC

### SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ $t_f$	Turn-off Delay Time Fall Time	$V_{DD} = 200 \text{ V}, I_D = 2.7\text{A}$ $R_G = 4.7\Omega, V_{GS} = 10 \text{ V}$ (Resistive Load see, Figure 3)		30 12		ns ns
$t_{r(Voff)}$ $t_f$ $t_c$	Off-voltage Rise Time Fall Time Cross-over Time	$V_{DD} = 320\text{V}, I_D = 5.4\text{A},$ $R_G = 4.7\Omega, V_{GS} = 10\text{V}$ (Inductive Load see, Figure 5)		12 10 20		ns ns ns

### SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM(2)}$	Source-drain Current Source-drain Current (pulsed)				5.4 21.6	A A
$V_{SD}(1)$	Forward On Voltage	$I_{SD} = 5.4 \text{ A}, V_{GS} = 0$			1.6	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 5.4 \text{ A}, di/dt = 100\text{A}/\mu\text{s}$ $V_{DD} = 50\text{V}, T_j = 150^\circ\text{C}$ (see test circuit, Figure 5)		220 990 9		ns nC A

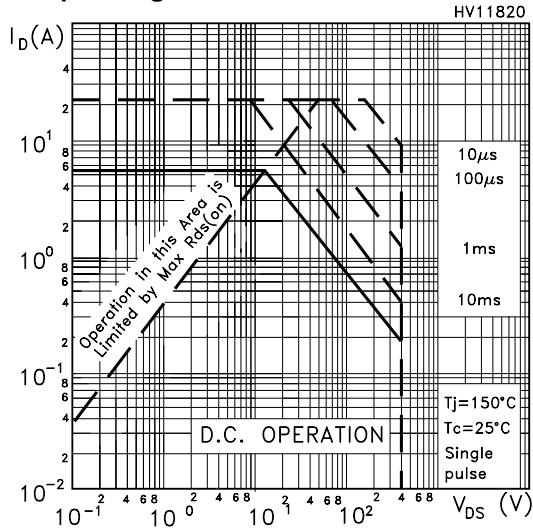
Note: 1. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %.

2. Pulse width limited by safe operating area.

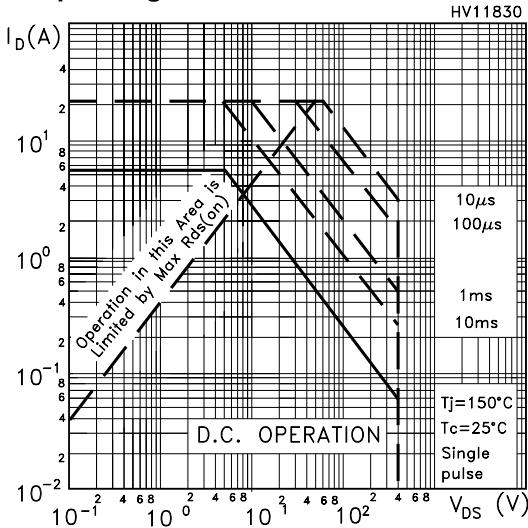
3.  $C_{oss \text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V$

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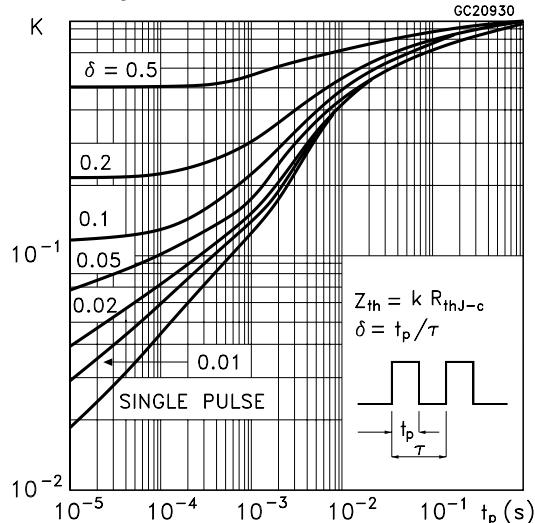
### Safe Operating Area For TO-220/DPAK/IPAK



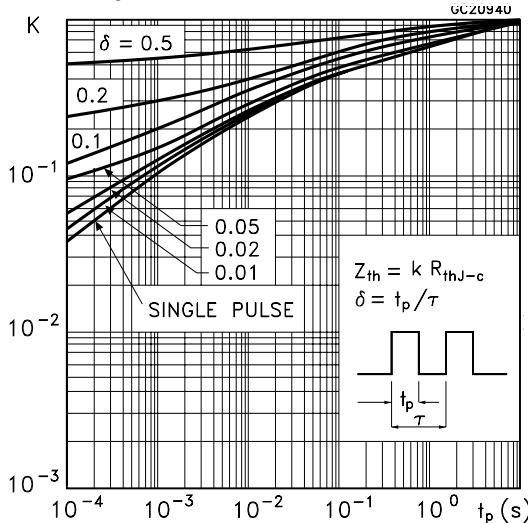
### Safe Operating Area For TO-220FP



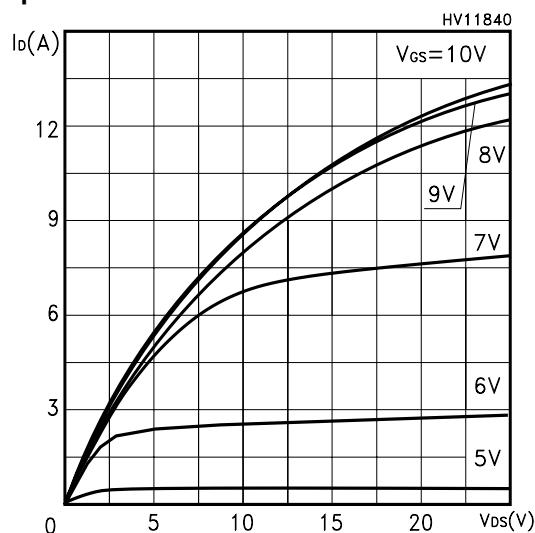
### Thermal Impedance For TO-220/DPAK/IPAK



### Thermal Impedance For TO-220FP



### Output Characteristics



### Transfer Characteristics

