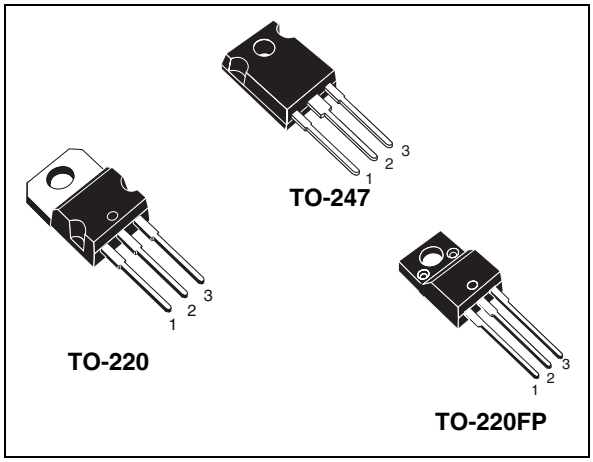
STF7N95K3
STP7N95K3, STW7N95K3

N-channel 950 V, 1.1 Ω, 7.2 A, TO-220, TO-220FP, TO-247
Zener-protected SuperMESH3™ Power MOSFET

Features

Type	V_{DSS}	$R_{DS(on)}$ max	I_D	Pw
STF7N95K3	950 V	< 1.35 Ω	7.2 A	35 W
STP7N95K3	950 V	< 1.35 Ω	7.2 A	150 W
STW7N95K3	950 V	< 1.35 Ω	7.2 A	150 W

- 100% avalanche tested
- Extremely large avalanche performance
- Gate charge minimized
- Very low intrinsic capacitances
- Zener-protected



Application

- Switching applications

Description

The new SuperMESH3™ series is obtained through the combination of a further fine tuning of ST's well established strip-based PowerMESH™ layout with a new optimized vertical structure. In addition to pushing on-resistance significantly down, special attention has been taken to ensure a very good dynamic performances coupled with a very large avalanche capability for the most demanding application.

Figure 1. Internal schematic diagram

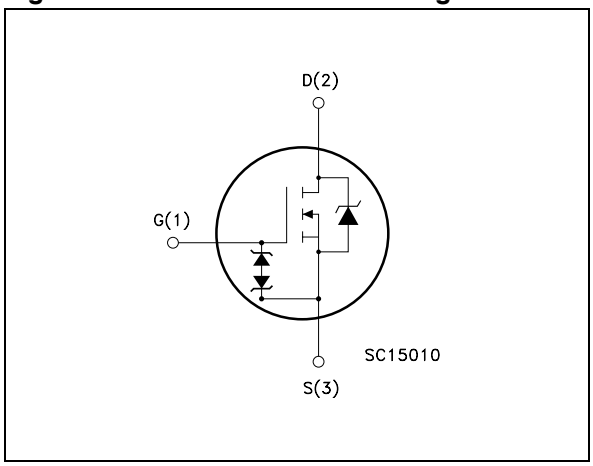


Table 1. Device summary

Order codes	Marking	Package	Packaging
STF7N95K3	7N95K3	TO-220FP	Tube
STP7N95K3	7N95K3	TO-220	Tube
STW7N95K3	7N95K3	TO-247	Tube

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220, TO-247	TO-220FP	
V_{GS}	Gate-source voltage	± 30		V
I_D	Drain current (continuous) at T_C = 25 °C	7.2	7.2 (1)	A
I_D	Drain current (continuous) at T_C = 100 °C	4.5	4.5 (1)	A
I_{DM} (2)	Drain current (pulsed)	28.8	28.8 (1)	A
P_{TOT}	Total dissipation at T_C = 25 °C	150	35	W
I_{AR}	Max current during repetitive or single pulse avalanche (pulse width limited by T_{JMAX})	9		A
E_{AS}	Single pulse avalanche energy (3)	220		mJ
	Derating factor	1.12	0.24	W/°C
dv/dt (4)	Peak diode recovery voltage slope	6		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s;T_C=25 °C)		2000	V
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 150		°C

1. Limited by package
2. Pulse width limited by safe operating area
3. Starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V
4. $I_{SD} \leq$ 7.2 A, di/dt = 100 A/µs, $V_{Peak} < V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	TO-220	TO-247	TO-220FP	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	0.83		3.57	°C/W
$Rt_{hj\text{-}amb}$	Thermal resistance junction-ambient max	62.5	50	62.5	°C/W
T_l	Maximum lead temperature for soldering purpose	300			°C

2 Electrical characteristics

(Tcase = 25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	950			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating V_{DS} = Max rating, T_C=125 °C			1 50	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 3.6 A		1.1	1.35	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 15 V, I_D = 3.6 A		5		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0		1031 79 0.9		pF pF pF
$C_{o(tr)}$(2)	Equivalent capacitance time related	V_{DS} = 0 to 760 V, V_{GS} = 0		60		pF
$C_{o(er)}$(3)	Equivalent capacitance energy related	V_{DS} = 0 to 760 V, V_{GS} = 0		36		pF
R_G	Gate input resistance	f=1 MHz Gate DC Bias=0 Test signal level = 20 mV open drain		2.4		Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 760 V, I_D = 7.2 A, V_{GS} = 10 V		34 6 20		nC nC nC

1. Pulsed: pulse duration = 300 µs, duty cycle 1.5%
2. $C_{oss\ eq.}$ time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
3. $C_{oss\ eq.}$ energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 475 V, I_D = 3.6 A, R_G = 4.7 Ω, V_{GS} = 10 V		14		ns
t_r	Rise time			9		ns
$t_{d(off)}$	Turn-off-delay time			36		ns
t_f	Fall time			23		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current				7.2	A
I_{SDM} (1)	Source-drain current (pulsed)				28.8	A
V_{SD} (2)	Forward on voltage	I_{SD} = 7.2 A, V_{GS} = 0			1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 7.2 A, di/dt = 100A/µs V_{DD} = 60 V (see		450		ns
Q_{rr}	Reverse recovery charge			6		µC
I_{RRM}	Reverse recovery current			28		A
t_{rr}	Reverse recovery time	I_{SD} = 7.2 A, di/dt = 100 A/µs V_{DD} = 60 V, T_j = 150 °C		550		ns
Q_{rr}	Reverse recovery charge			8		µC
I_{RRM}	Reverse recovery current			28		A

1. Pulse width limited by safe operating area
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BV_{GSO} (1)	Gate-source breakdown voltage	Igs=± 1mA (open drain)	30			V

1. The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220

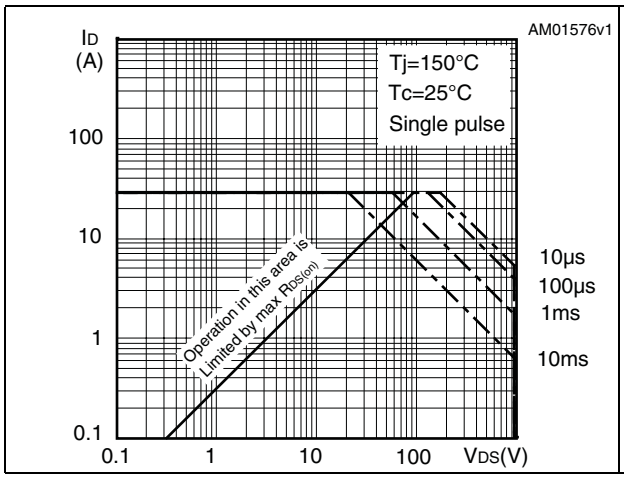


Figure 3. Thermal impedance for TO-220

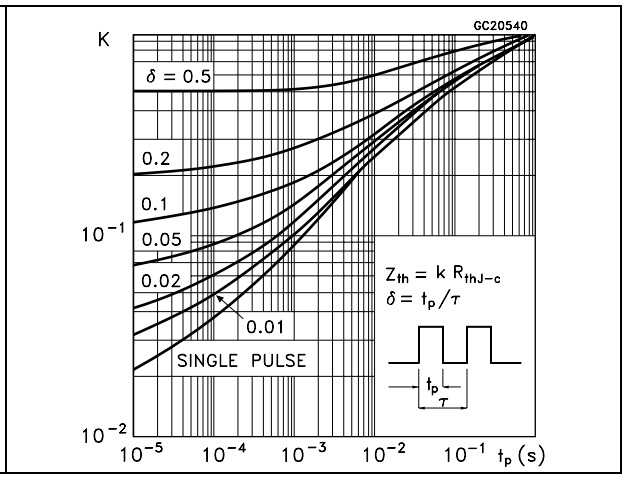


Figure 4. Safe operating area for TO-220FP

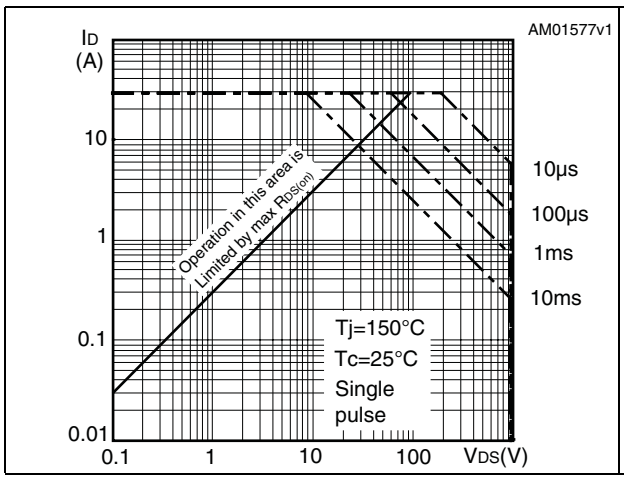


Figure 5. Thermal impedance for TO-220FP

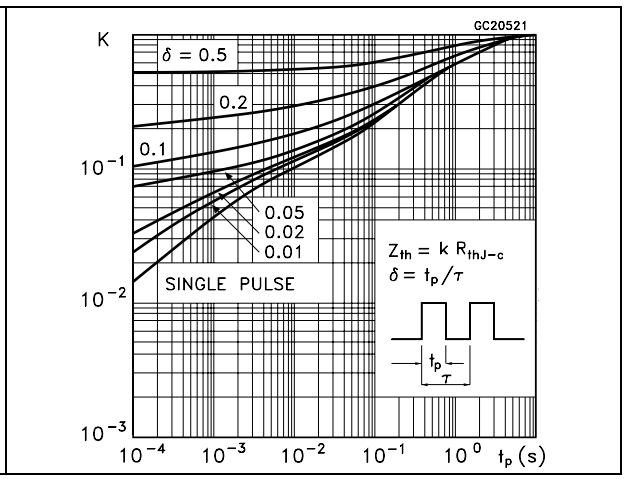


Figure 6. Safe operating area for TO-247

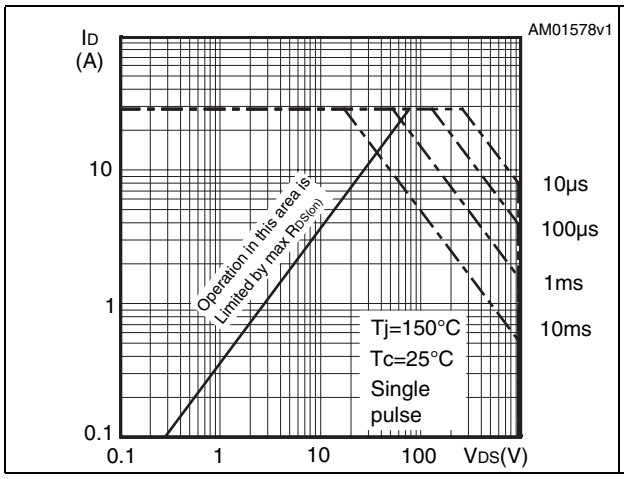


Figure 7. Thermal impedance for TO-247