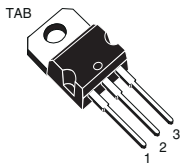
STP77N6F6

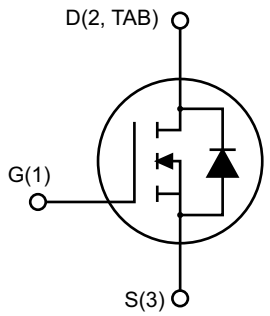
N-channel 60 V, 0.0063 Ω typ., 77 A STripFET™ VI DeepGATE™ Power MOSFET in a TO-220 package

Datasheet — production data



TO-220

Figure 1. Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max	I_D	P_{TOT}
STP77N6F6	60 V	0.007 Ω	77 A	80 W

- $R_{DS(on)}$ * Q_g industry benchmark
- Extremely low on-resistance $R_{DS(on)}$
- High avalanche ruggedness
- Low gate drive power losses
- Very low switching gate charge

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the 6th generation of STripFET™ DeepGATE™ technology, with a new gate structure. The resulting Power MOSFET exhibits the lowest $R_{DS(on)}$ in all packages.

Table 1. Device summary

Order code	Marking	Package	Packaging
STP77N6F6	77N6F6	TO-220	Tube

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	60	V
V_{GS}	Gate-source voltage	±20	V
I_D(1)	Drain current (continuous) at T_c = 25 °C	77	A
I_D(1)	Drain current (continuous) at T_c = 100 °C	55	A
I_{DM}(2)	Drain current (pulsed)	308	A
P_{TOT}(1)	Total dissipation at T_c = 25 °C	80	W
$T_{J\ Pstg}$	Operating junction temperature storage temperature	-55 to 175	°C

1. This value is rated according to R_{thj-c}
2. Pulse width is limited by safe operating area

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thj-c}	Thermal resistance junction-case	1.88	°C/W
R_{thj-a}(1)	Thermal resistance junction-ambient	62.5	

1. When mounted on FR-4 board of 1 inch², 2 oz Cu, t < 10 sec

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AV}	Avalanche current, repetitive or not-repetitive (pulse width limited by maximum junction temperature)	38.5	A
E_{AS}	Single pulse avalanche energy (T_J = 25 °C, I_D = I_{AV}, V_{DD} = 43 V)	152	mJ

2 Electrical characteristics

(T_J= 25 °C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS} = 0	60			V
I_{DSS}	Zero gate voltage Drain current	V_{DS} = 60 V, V_{GS} = 0			10	µA
		V_{DS} = 60 V, V_{GS}= 0, T_J=125 °C			100	µA
I_{GSS}	Gate-body leakage current	V_{GS} = ± 20 V, V_{DS} = 0			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 38.5 A		0.0063	0.007	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0	-	4295	-	pF
C_{oss}	Output capacitance		-	292	-	pF
C_{rss}	Reverse transfer capacitance		-	190	-	pF
Q_g	Total gate charge	V_{DD} = 30 V, I_D = 77 A, V_{GS} = 10 V	-	70.5	-	nC
Q_{gs}	Gate-source charge		-	19.7	-	nC
Q_{gd}	Gate-drain charge		-	16.2	-	nC
R_g	Intrinsic gate resistance	f = 1 MHz open drain	-	2.2	-	Ω

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 30 V, I_D = 77 A R_G = 4.7 Ω V_{GS} = 10 V	-	22	-	ns
t_r	Rise time		-	42	-	ns
$t_{d(off)}$	Turn-off-delay time		-	73	-	ns
t_f	Fall time		-	16	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		77	A
I_{SDM} (1)	Source-drain current (pulsed)		-		308	A
V_{SD} (2)	Forward on voltage	I_{SD} = 77 A, V_{GS} = 0	-		1.3	V
t_{rr}	Reverse recovery time	I_{SD} = 77 A, V_{DD} = 48 V di/dt = 100 A/µs, T_j = 25 °C	-	49		ns
Q_{rr}	Reverse recovery charge		-	8.5		nC
I_{RRM}	Reverse recovery current		-	0.3		A

1. Pulse width is limited by safe operating area
2. Pulse test: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

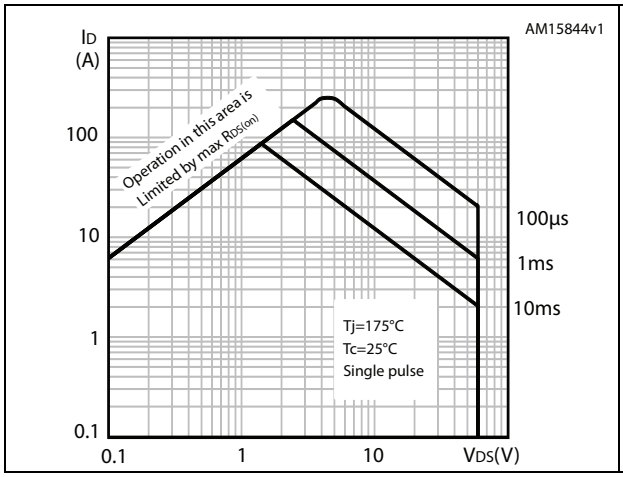


Figure 3. Thermal impedance

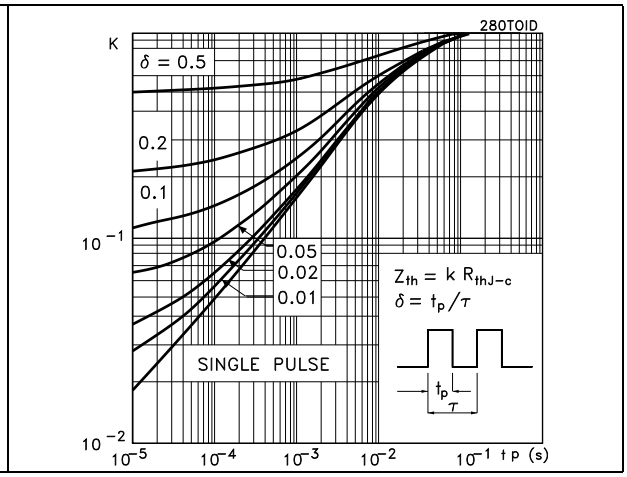


Figure 4. Output characteristics

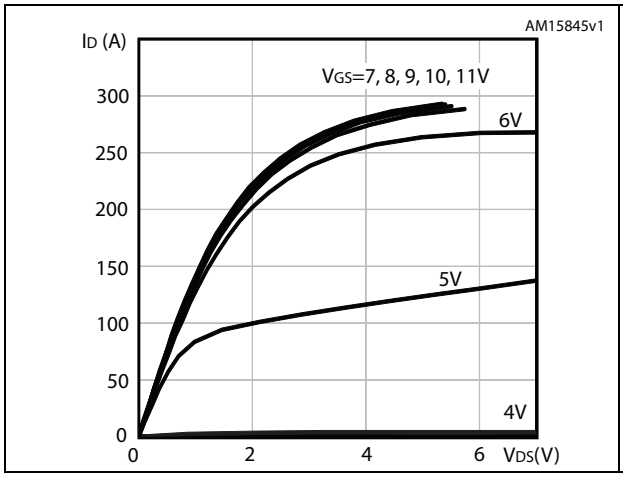


Figure 5. Transfer characteristics

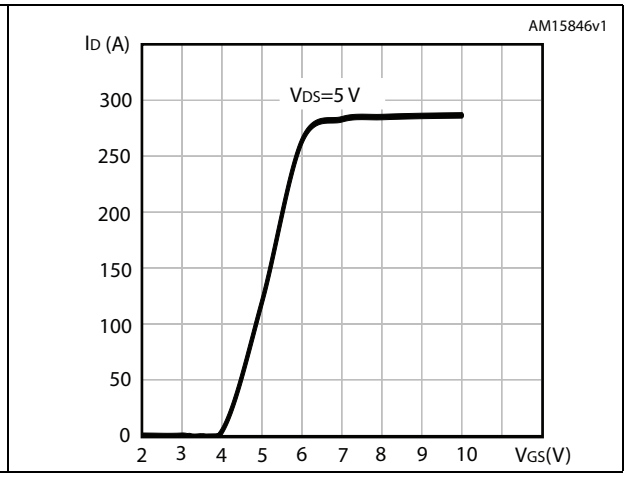


Figure 6. Gate charge vs gate-source voltage

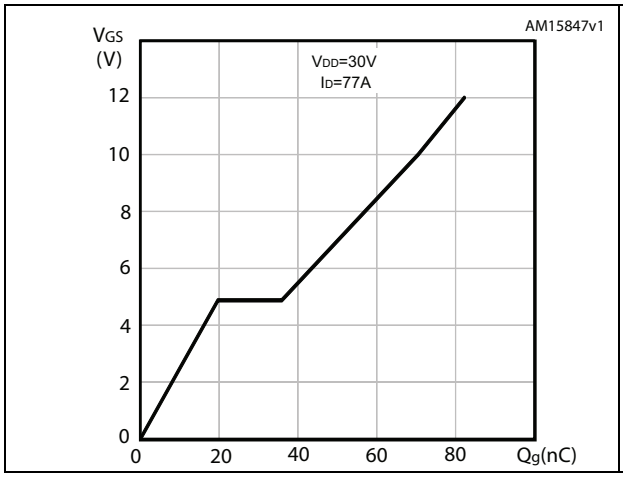


Figure 7. Static drain-source on-resistance