STP75N75F4

N-channel 75 V, 0.0092 Ω typ., 78 A STripFET™ DeepGATE™ Power MOSFET in a TO-220 package

Datasheet — production data

Features

Type	V_{DSS}	$R_{DS(on)}$ max	I_D
STP75N75F4	75 V	< 0.011 Ω	78 A

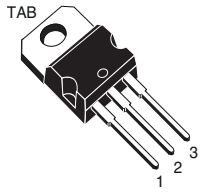
- N-channel enhancement mode
- 100% avalanched rated
- Low gate charge
- Very low on-resistance

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using ST's STripFET™ DeepGATE™ technology. The device has a new gate structure and is specially designed to minimize on-state resistance to provide superior switching performance.



TO-220

Figure 1. Internal schematic diagram

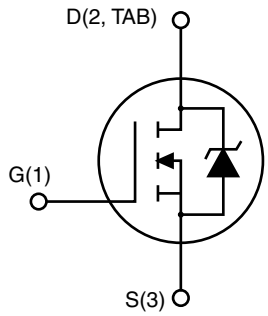


Table 1. Device summary

Order codes	Marking	Package	Packaging
STP75N75F4	75N75F4	TO-220	Tube

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	75	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at T_C = 25 °C	78	A
I_D	Drain current (continuous) at T_C = 100 °C	55	A
I_{DM} (1)	Drain current (pulsed)	312	A
P_{TOT}	Total dissipation at T_C = 25 °C	150	W
	Derating factor	1	W/°C
E_{AS} (2)	Single pulse avalanche energy	185	mJ
T_{stg}	Storage temperature	– 55 to 175	°C
T_j	Operating junction temperature		

1. Pulse width limited by safe operating area
2. Starting T_j = 25 °C, I_D= 35 A, V_{DD}= 50 V

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	1	°C/W
$R_{thj\text{-}a}$	Thermal resistance junction-ambient max	62.5	°C/W

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown voltage	I_D = 250 µA, V_{GS} = 0	75			V
I_{DSS}	Zero gate voltage Drain current (V_{GS} = 0)	V_{DS} = 75 V V_{DS} = 75 V,T_C=125 °C			1 100	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 39 A		0.0092	0.011	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0	-	5015	-	pF
C_{oss}	Output capacitance			382		pF
C_{rss}	Reverse transfer capacitance			218		pF
Q_g	Total gate charge	V_{DD} = 37.5 V, I_D = 78 A, V_{GS} = 10 V	-	76	-	nC
Q_{gs}	Gate-source charge			23		nC
Q_{gd}	Gate-drain charge			18.5		nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	V_{DD} = 37.5 V, I_D = 39 A R_G = 4.7 Ω V_{GS} = 10 V	-	25 33	-	ns ns
$t_{d(off)}$ t_f	Turn-off-delay time Fall time		-	61 14	-	ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current		-		78	A
I_{SDM} (1)	Source-drain current (pulsed)		-		312	A
V_{SD} (2)	Forward on voltage	I_{SD} = 78 A, V_{GS} = 0	-		1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 78 A, V_{DD} = 60 V di/dt = 100 A/µs, T_j = 150 °C	-	67 183 5.5		ns nC A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

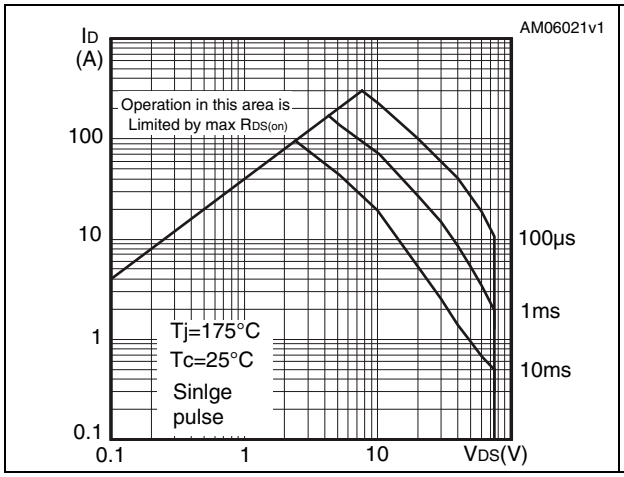


Figure 3. Thermal impedance

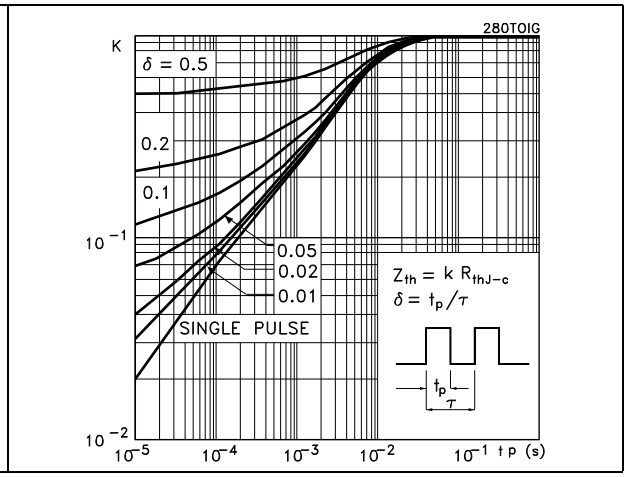


Figure 4. Output characteristics

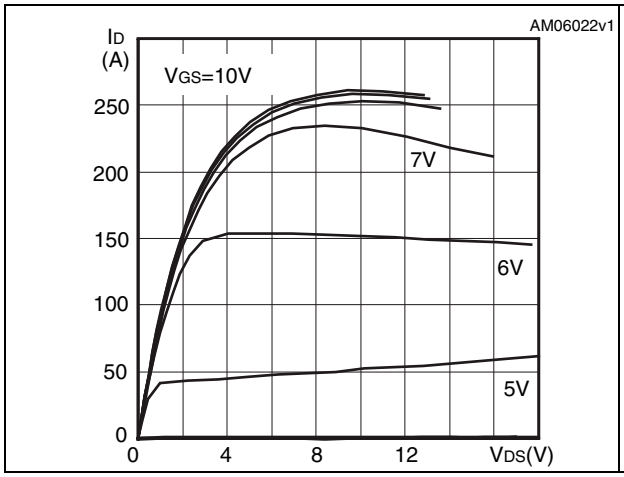


Figure 5. Transfer characteristics

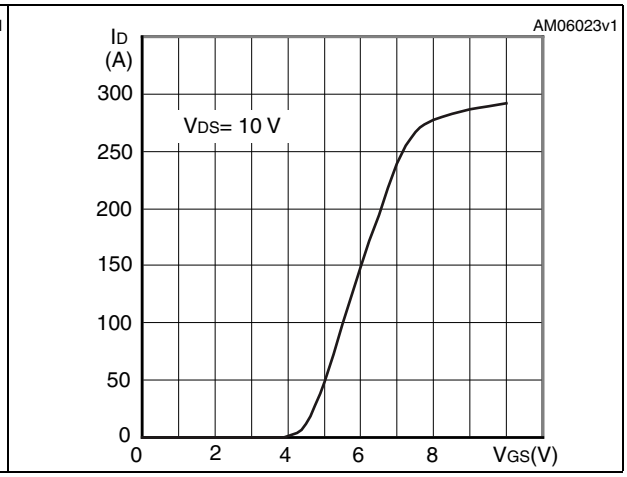


Figure 6. Normalized BV_{DSS} vs temperature

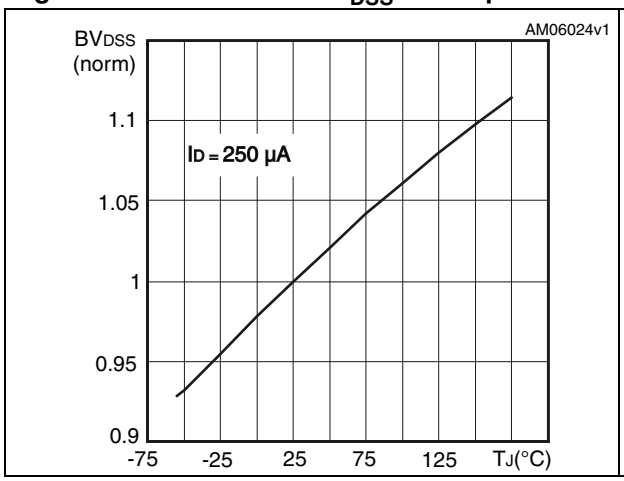


Figure 7. Static drain-source on-resistance