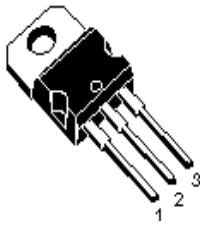
STP6NK50Z - STF6NK50Z
STD6NK50Z

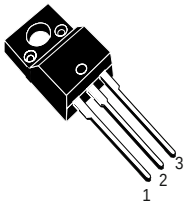
N-CHANNEL 500V - 0.93Ω - 5.6A TO-220/TO-220FP/DPAK
Zener-Protected SuperMESH™ MOSFET

TYPE	V_{DSS}	$R_{DS(on)}$	I_D	Pw
STP6NK50Z	500 V	< 1.2 Ω	5.6 A	90 W
STF6NK50Z	500 V	< 1.2 Ω	5.6 A	25 W
STD6NK50Z	500 V	< 1.2 Ω	5.6 A	90 W

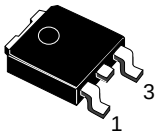
- TYPICAL $R_{DS}(on)$ = 0.93 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- GATE CHARGE MINIMIZED
- VERY LOW INTRINSIC CAPACITANCES
- VERY GOOD MANUFACTURING REPEATIBILITY



TO-220



TO-220FP

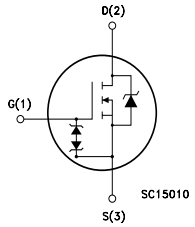


DPAK

DESCRIPTION

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

INTERNAL SCHEMATIC DIAGRAM



APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- IDEAL FOR OFF-LINE POWER SUPPLIES, ADAPTORS AND PFC
- LIGHTING

ORDER CODES

PART NUMBER	MARKING	PACKAGE	PACKAGING
STP6NK50Z	P6NK50Z	TO-220	TUBE
STF6NK50Z	F6NK50Z	TO-220FP	TUBE
STD6NK50ZT4	D6NK50Z	DPAK	TAPE & REEL

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		STP6NK50Z STD6NK50Z	STF6NK50Z	
V_{DS}	Drain-source Voltage (V_{GS} = 0)	500		V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	500		V
V_{GS}	Gate- source Voltage	± 30		V
I_D	Drain Current (continuous) at T_C = 25°C	5.6	5.6 (*)	A
I_D	Drain Current (continuous) at T_C = 100°C	3.5	3.5 (*)	A
I_{DM} (•)	Drain Current (pulsed)	22.4	22.4 (*)	A
P_{TOT}	Total Dissipation at T_C = 25°C	90	25	W
	Derating Factor	0.72	0.2	W/°C
$V_{ESD(G-S)}$	Gate source ESD(HBM-C=100pF, R=1.5KΩ)	3000		V
dv/dt (1)	Peak Diode Recovery voltage slope	4.5		V/ns
V_{ISO}	Insulation Withstand Voltage (DC)	-	2500	V
T_j T_{stg}	Operating Junction Temperature Storage Temperature	-55 to 150		°C

(•) Pulse width limited by safe operating area
(1) $I_{SD} \leq 5.6A$, $di/dt \leq 200$ A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$.
(*) Limited only by maximum temperature allowed

THERMAL DATA

		TO-220 DPAK	TO-220FP	
Rthj-case	Thermal Resistance Junction-case Max	1.38	5	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	62.5		°C/W
T_l	Maximum Lead Temperature For Soldering Purpose	300		°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	5.6	A
E_{AS}	Single Pulse Avalanche Energy (starting T_j = 25 °C, $I_D = I_{AR}$, V_{DD} = 50 V)	180	mJ

GATE-SOURCE ZENER DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-Source Breakdown Voltage	Igs=± 1mA (Open Drain)	30			V

PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

ELECTRICAL CHARACTERISTICS (T_{CASE} =25°C UNLESS OTHERWISE SPECIFIED)

ON/OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 1 mA, V_{GS} = 0	500			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating, T_C = 125 °C			1 50	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 20V			±10	µA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 50µA	3	3.75	4.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10V, I_D = 2.8 A		0.93	1.2	Ω

DYNAMIC

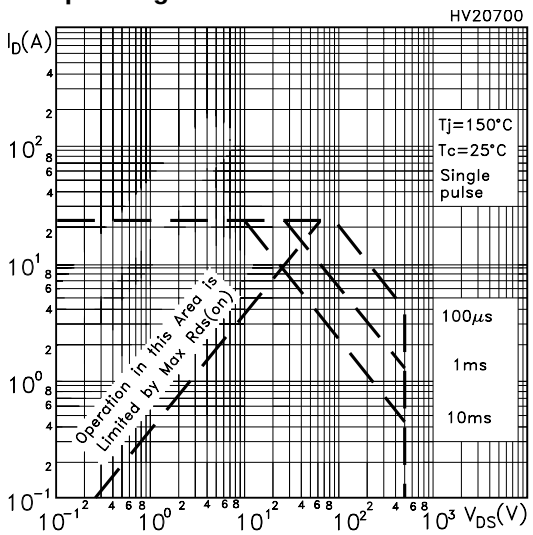
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	V_{DS} = 8 V, I_D = 2.8 A		4.3		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		690 100 20		pF pF pF
$C_{oss\ eq.}$ (3)	Equivalent Output Capacitance	V_{GS} = 0V, V_{DS} = 0V to 400V		52		pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on Delay Time Rise Time Turn-off Delay Time Fall Time	V_{DD} = 250 V, I_D = 2.8 A R_G = 4.7Ω V_{GS} = 10 V (Resistive Load see, Figure 3)		12 23.5 31 23		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD} = 400V, I_D = 5.6 A, V_{GS} = 10V		24.6 4.9 13.3		nC nC nC

SOURCE DRAIN DIODE

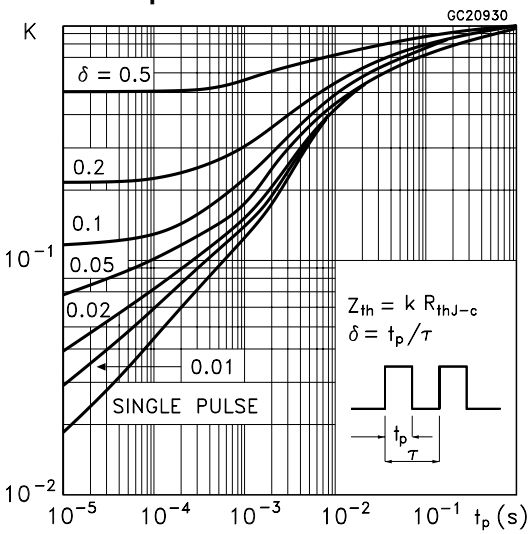
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (2)	Source-drain Current Source-drain Current (pulsed)				5.6 22.4	A A
V_{SD} (1)	Forward On Voltage	I_{SD} = 5.6 A, V_{GS} = 0			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 5.6 A, di/dt = 100 A/µs V_{DD} = 48V, T_j = 25°C (see test circuit, Figure 5)		254 1.2 10		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 5.6 A, di/dt = 100 A/µs V_{DD} = 48V, T_j = 150°C (see test circuit, Figure 5)		360 1.9 11		ns µC A

Note: 1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
2. Pulse width limited by safe operating area.
3. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

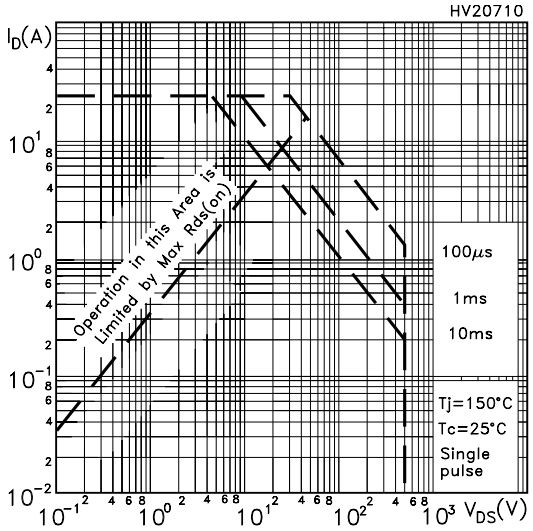
Safe Operating Area for TO-220



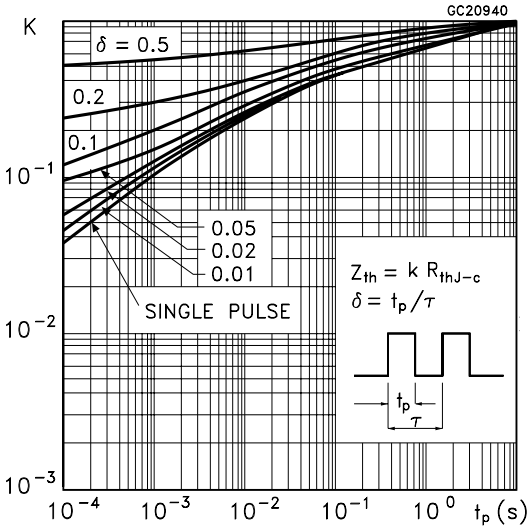
Thermal Impedance for TO-220



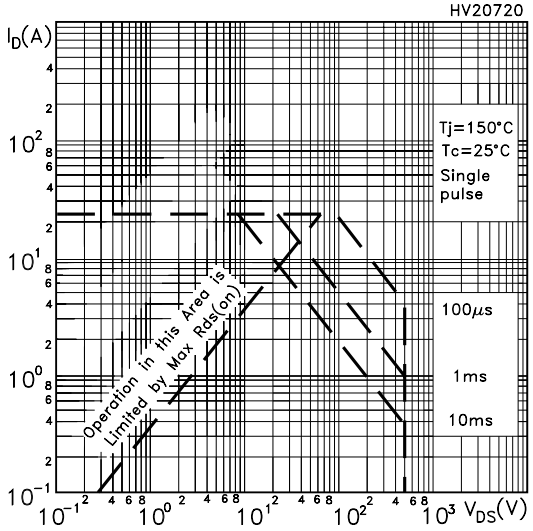
Safe Operating Area for TO-220FP



Thermal Impedance for TO-220FP



Safe Operating Area for DPAK



Thermal Impedance for DPAK