

# **STD6N95K5, STF6N95K5, STP6N95K5, STW6N95K5, STU6N95K5**

N-channel 950 V, 1 Ω typ., 9 A Zener-protected SuperMESH™ 5 Power MOSFET in DPAK, TO-220FP, TO-220, TO-247 and IPAK

Datasheet — production data

## Features

Type	V <sub>DSS</sub>	R <sub>DS(on)max.</sub>	I <sub>D</sub>	P <sub>W</sub>
STD6N95K5	950 V	< 1.25 Ω	9 A	90 W
STF6N95K5			9 A	25 W
STP6N95K5			9 A	90 W
STW6N95K5			9 A	90 W
STU6N95K5				

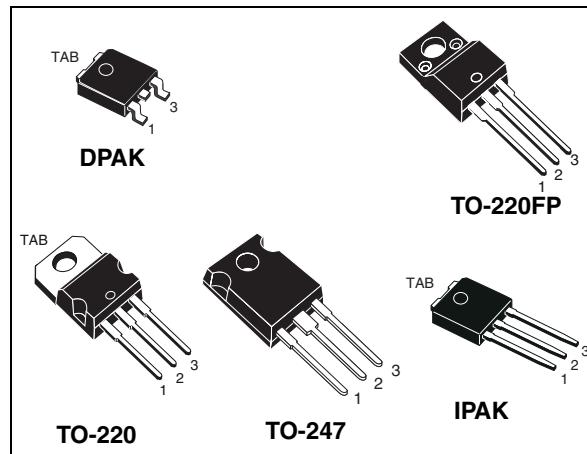
- DPAK 950 V worldwide best R<sub>DS(on)</sub>
- Worldwide best FOM (figure of merit)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected

## Applications

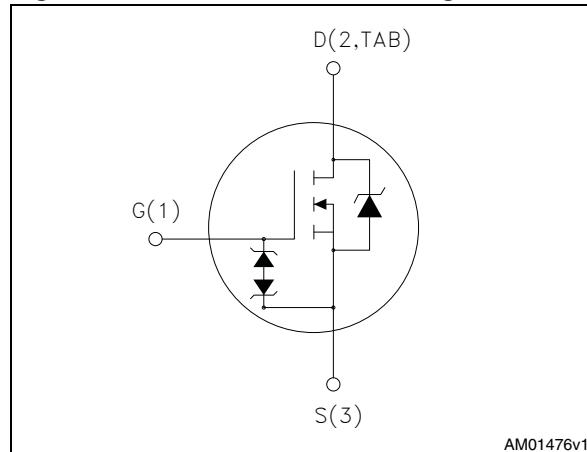
- Switching applications

## Description

These devices are N-channel Power MOSFETs developed using SuperMESH™ 5 technology. This revolutionary, avalanche-rugged, high voltage Power MOSFET technology is based on an innovative proprietary vertical structure. The result is a drastic reduction in on-resistance and ultra low gate charge for applications which require superior power density and high efficiency.



**Figure 1. Internal schematic diagram**



**Table 1. Device summary**

Order codes	Marking	Package	Packaging
STD6N95K5	6N95K5	DPAK	Tape and reel
STF6N95K5		TO-220FP	
STP6N95K5		TO-220	
STW6N95K5		TO-247	Tube
STU6N95K5		IPAK	

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value		Unit
		TO-220, DPAK TO-247, IPAK	TO-220FP	
$V_{GS}$	Gate- source voltage	$\pm 30$		V
$I_D$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	9	9 <sup>(1)</sup>	A
$I_D$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	6	6 <sup>(1)</sup>	A
$I_{DM}^{(2)}$	Drain current (pulsed)	36	36 <sup>(1)</sup>	A
$P_{TOT}$	Total dissipation at $T_C = 25^\circ\text{C}$	90	25	W
$I_{AR}^{(3)}$	Max current during repetitive or single pulse avalanche	3		A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25^\circ\text{C}$ , $I_D=I_{AS}$ , $V_{DD}= 50\text{ V}$ )	90		mJ
$V_{ISO}$	Insulation withstand voltage (RMS) from all three leads to external heat sink ( $t=1\text{ s}; T_C=25^\circ\text{C}$ )	2500		V
$dv/dt^{(4)}$	Peak diode recovery voltage slope	4.5		V/ns
$T_j$ $T_{stg}$	Operating junction temperature Storage temperature	- 55 to 150		°C

1. Limited by package.
2. Pulse width limited by safe operating area.
3. Pulse width limited by  $T_{Jmax}$ .
4.  $I_{SD} \leq 9\text{ A}$ ,  $di/dt \leq 100\text{ A}/\mu\text{s}$ ,  $V_{Peak} \leq V_{(BR)DSS}$

**Table 3. Thermal data**

Symbol	Parameter	Value				Unit
		TO-220 IPAK	DPAK	TO-247	TO-220FP	
$R_{thj-case}$	Thermal resistance junction-case max	1.39		5	5	°C/W
$R_{thj-amb}$	Thermal resistance junction-amb max	62.5		50	62.5	°C/W
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max	50				°C/W

1. When mounted on 1inch<sup>2</sup> FR-4 board, 2 oz Cu

## 2 Electrical characteristics

( $T_{CASE} = 25^\circ\text{C}$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1 \text{ mA}, V_{GS}=0$	950			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 950 \text{ V}$ $V_{DS} = 950 \text{ V}, T_c=125^\circ\text{C}$			1 50	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20 \text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(\text{th})}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 100 \mu\text{A}$	3	4	5	V
$R_{DS(\text{on})}$	Static drain-source on-resistance	$V_{GS} = 10 \text{ V}, I_D = 3 \text{ A}$		1	1.25	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance			450		pF
$C_{oss}$	Output capacitance		-	30	-	pF
$C_{rss}$	Reverse transfer capacitance	$V_{DS} = 100 \text{ V}, f=1 \text{ MHz}, V_{GS}=0$		1.6		pF
$C_{o(\text{tr})}^{(1)}$	Equivalent capacitance time related	$V_{GS} = 0, V_{DS} = 0 \text{ to } 760 \text{ V}$	-	45	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related		-	19	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{MHz open drain}$	-	7	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 760 \text{ V}, I_D = 6 \text{ A}$		13		nC
$Q_{gs}$	Gate-source charge	$V_{GS} = 10 \text{ V}$	-	3	-	nC
$Q_{gd}$	Gate-drain charge			7		nC

1. Time related is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$
2. energy related is defined as a constant equivalent capacitance giving the same stored energy as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 475 \text{ V}, I_D = 3 \text{ A}, R_G=4.7 \Omega, V_{GS}=10 \text{ V}$	-	12	-	ns
$t_r$	Rise time			12		ns
$t_{d(off)}$	Turn-off delay time			33		ns
$t_f$	Fall time			21		ns

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-	9	36	A
$I_{SDM}$	Source-drain current (pulsed)					A
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 6 \text{ A}, V_{GS}=0$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 6 \text{ A}, V_{DD}= 60 \text{ V}$ $di/dt = 100 \text{ A}/\mu\text{s},$	-	372	ns	$\mu\text{C}$
$Q_{rr}$	Reverse recovery charge			4		
$I_{RRM}$	Reverse recovery current			22		
$t_{rr}$	Reverse recovery time	$I_{SD} = 6 \text{ A}, V_{DD}= 60 \text{ V}$ $di/dt=100 \text{ A}/\mu\text{s},$ $T_j=150^\circ\text{C}$	-	522	ns	$\mu\text{C}$
$Q_{rr}$	Reverse recovery charge			5		
$I_{RRM}$	Reverse recovery current			20		

1. Pulsed: pulse duration = 300 $\mu\text{s}$ , duty cycle 1.5%

**Table 8. Gate-source Zener diode**

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} \pm 1\text{mA}, I_D = 0$	30	-		V

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220FP

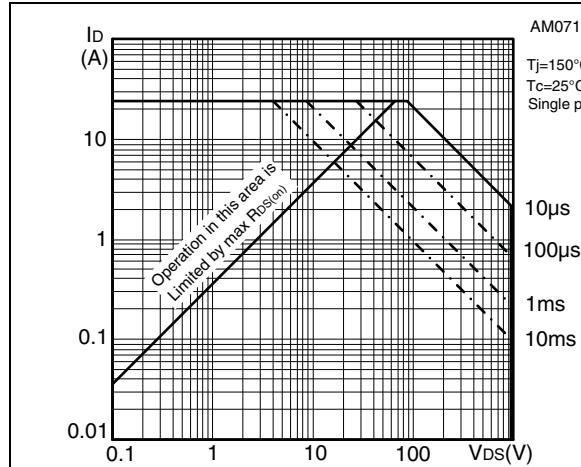


Figure 3. Thermal impedance for TO-220FP

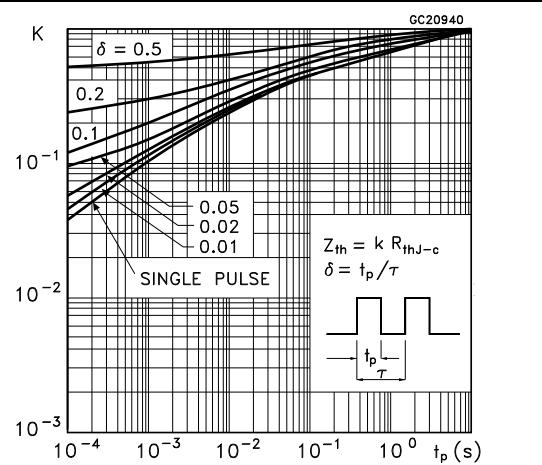


Figure 4. Safe operating area for TO-220 and TO-247

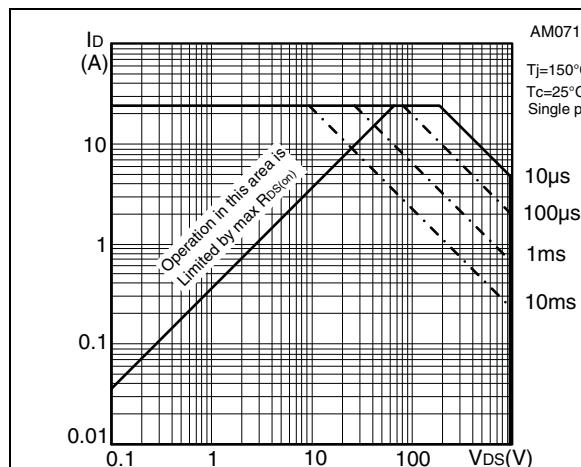


Figure 5. Thermal impedance for TO-220 and TO-247

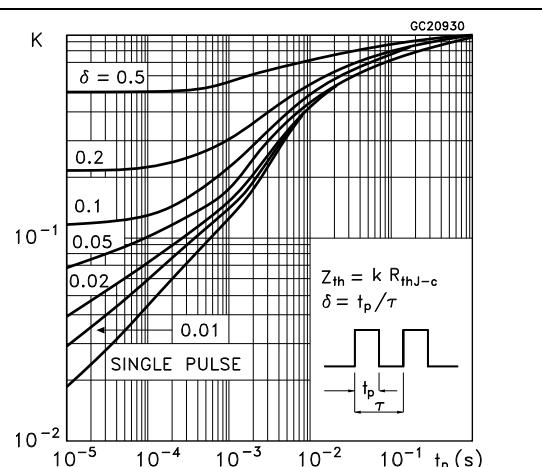


Figure 6. Safe operating area for DPAK and IPAK

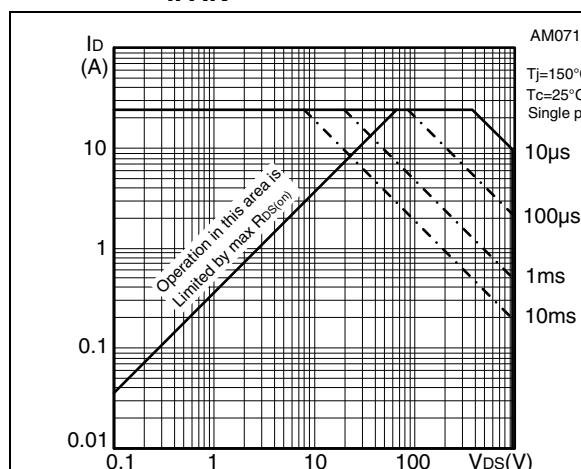


Figure 7. Thermal impedance for DPAK and IPAK

