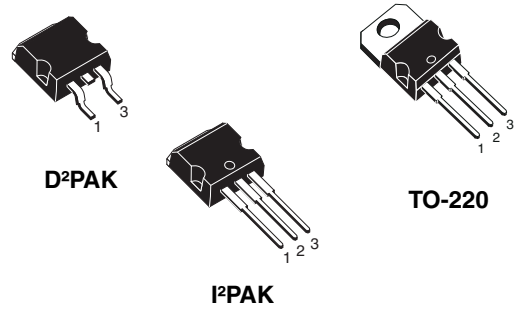
STB60NF10
STB60NF10-1 - STP60NF10

N-channel 100V - 0.019Ω - 80A - TO-220 - D²PAK - I²PAK
STripFET™ II Power MOSFET

General features

Type	V_{DSS} (@Tjmax)	$R_{DS(on)}$	I_D
STB60NF10	100V	<0.023Ω	80A
STB60NF10-1	100V	<0.023Ω	80A
STP60NF10	100V	<0.023Ω	80A

- Exceptional dv/dt capability
- 100% avalanche tested



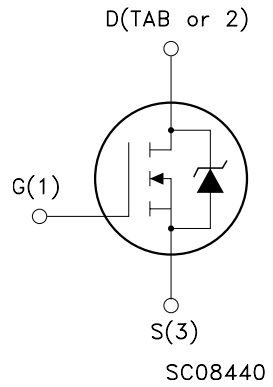
Description

This Power MOSFET series realized with STMicroelectronics unique STripFET™ process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced high-efficiency, high-frequency isolated DC-DC converters for Telecom and Computer applications. It is also intended for any applications with low gate drive requirements.

Applications

- Switching application

Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STB60NF10T4	B60NF10	D²PAK	Tape & reel
STB60NF10-1	B60NF10	I²PAK	Tube
STP60NF10	P60NF10	TO-220	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	100	V
V_{GS}	Gate-source voltage	± 20	V
I_D(1)	Drain current (continuous) at T_C = 25°C	80	A
I_D	Drain current (continuous) at T_C=100°C	66	A
I_{DM}(2)	Drain current (pulsed)	320	A
P_{TOT}	Total dissipation at T_C = 25°C	300	W
	Derating factor	2	W/°C
dv/dt (3)	Peak diode recovery voltage slope	16	V/ns
E_{AS} (4)	Single pulse avalanche energy	485	J
T_{stg}	Storage temperature	-55 to 175	°C

1. Current limited by package
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 80A$, di/dt $\leq 300A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq T_{JMAX}$
4. Starting T_J = 25 °C, I_D = 40A, V_{DD} = 30V

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance junction-case max	0.5	°C/W
R_{thJA}	Thermal resistance junction-ambient max	62.5	°C/W
T_l	Maximum lead temperature for soldering purpose	300	°C

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250µA, V_{GS}= 0	100			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating, V_{DS} = Max rating @125°C			1 10	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±20V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS}= 10V, I_D= 40A		0.019	0.023	Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 25V, I_D = 40A		78		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} =25V, f = 1 MHz, V_{GS} = 0		4270 470 140		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 50V, I_D = 80A V_{GS} =10V		104 20 32		nC nC nC

1. Pulsed: pulse duration=300µs, duty cycle 1.5%

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD}= 50V, I_D= 40A, R_G=4.7Ω, V_{GS}=10V		17 56 82 23		ns ns ns ns

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current				80	A
I_{SDM}(1)	Source-drain current (pulsed)				320	A
V_{SD}(2)	Forward on voltage	I_{SD} = 80A, V_{GS} = 0			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 80A, di/dt = 100A/µs, V_{DD} = 25V, T_J = 150°C		92 340 7.4		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

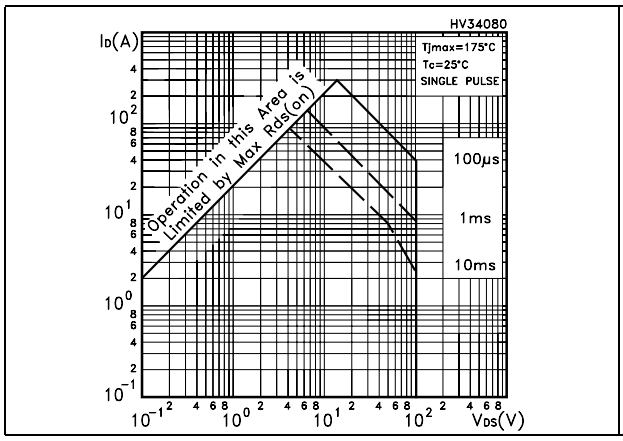


Figure 2. Thermal impedance

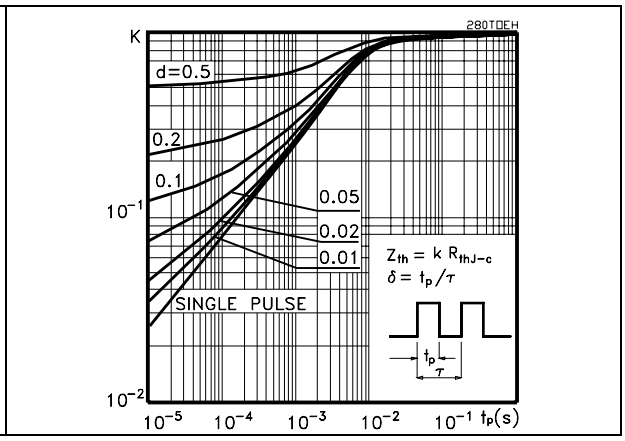


Figure 3. Output characterisics

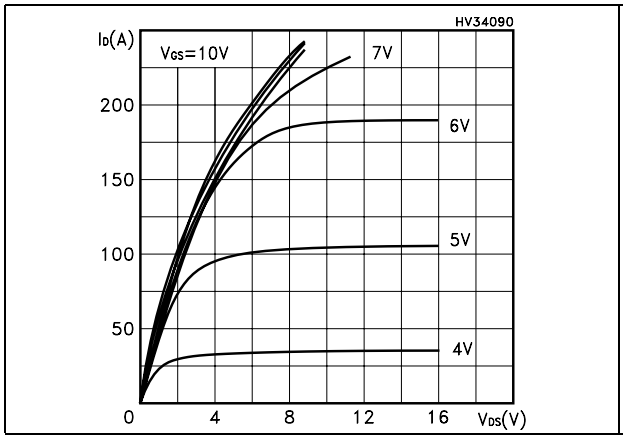


Figure 4. Transfer characteristics

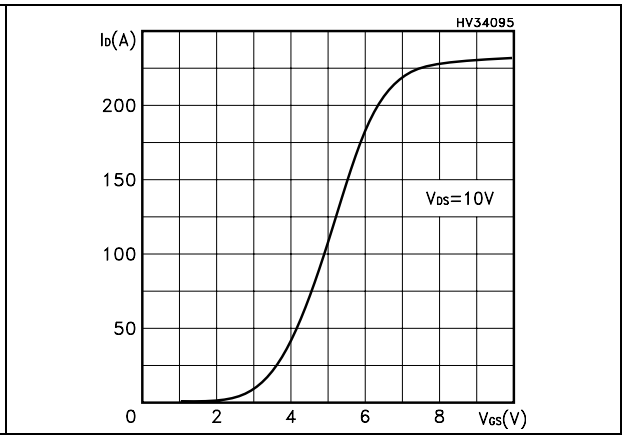


Figure 5. Transconductance

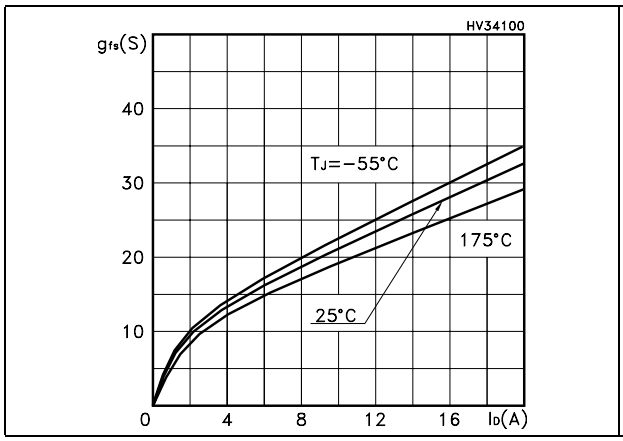


Figure 6. Static drain-source on resistance