

STD60N3LH5 STP60N3LH5, STU60N3LH5

N-channel 30 V, 0.0072 Ω , 48 A DPAK, IPAK, TO-220
STripFET™ V Power MOSFET

Features

Type	V_{DSS}	$R_{DS(on)}$ max	I_D
STD60N3LH5	30 V	0.008 Ω	48 A
STP60N3LH5	30 V	0.0084 Ω	48 A
STU60N3LH5	30 V	0.0084 Ω	48 A

- $R_{DS(on)} * Q_g$ industry benchmark
- Extremely low on-resistance $R_{DS(on)}$
- Very low switching gate charge
- High avalanche ruggedness
- Low gate drive power losses

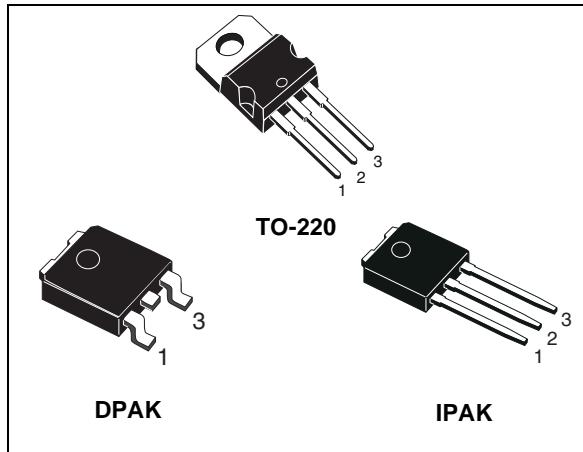
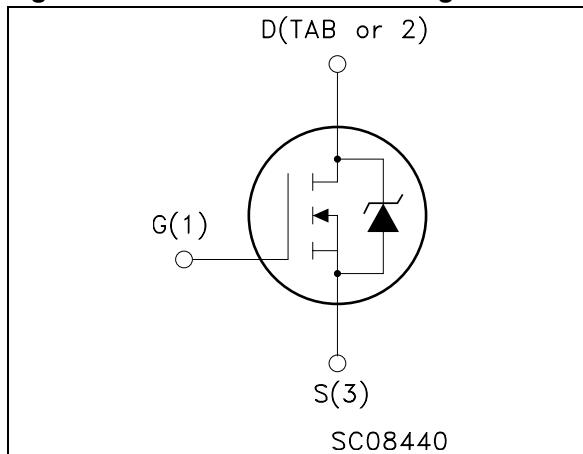


Figure 1. Internal schematic diagram



Application

- Switching applications

Description

This STripFET™V Power MOSFET technology is among the latest improvements, which have been especially tailored to achieve very low on-state resistance providing also one of the best-in-class FOM.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STD60N3LH5	60N3LH5	DPAK	Tape and reel
STP60N3LH5	60N3LH5	TO-220	Tube
STU60N3LH5	60N3LH5	IPAK	Tube

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS}=0$)	30	V
V_{DS}	Drain-source voltage ($V_{GS} = 0$) @ T_{JMAX}	35	V
V_{GS}	Gate-Source voltage	± 22	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25$ °C	48	A
I_D	Drain current (continuous) at $T_C = 100$ °C	42.8	A
$I_{DM}^{(2)}$	Drain current (pulsed)	192	A
P_{TOT}	Total dissipation at $T_C = 25$ °C	60	W
	Derating factor	0.4	W/°C
$E_{AS}^{(3)}$	Single pulse avalanche energy	160	mJ
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 175	°C

1. Limited by wire bonding
2. Pulse width limited by safe operating area
3. Starting $T_j = 25$ °C, $I_d = 24$ A, $Vdd = 12$ V

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	2.5	°C/W
$R_{thj-amb}$	Thermal resistance junction-case max	100	°C/W
T_j	Maximum lead temperature for soldering purpose	275	°C

2 Electrical characteristics

($T_{CASE} = 25^\circ\text{C}$ unless otherwise specified)

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0$	30			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 30 \text{ V}$ $V_{DS} = 30 \text{ V}, T_c = 125^\circ\text{C}$			1 10	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 22 \text{ V}$			± 100	nA
$V_{GS(\text{th})}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	1	1.8	3	V
$R_{DS(\text{on})}$	Static drain-source on resistance	$V_{GS} = 10 \text{ V}, I_D = 24 \text{ A}$ SMD version		0.0072	0.008	Ω
		$V_{GS} = 10 \text{ V}, I_D = 24 \text{ A}$		0.0076	0.0084	Ω
		$V_{GS} = 5 \text{ V}, I_D = 24 \text{ A}$ SMD version		0.0088	0.011	Ω
		$V_{GS} = 5 \text{ V}, I_D = 24 \text{ A}$		0.0092	0.0114	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance					pF
C_{oss}	Output capacitance					pF
C_{rss}	Reverse transfer capacitance	$V_{DS} = 25 \text{ V}, f = 1 \text{ MHz}, V_{GS} = 0$	-	1350 265 32	-	pF
Q_g	Total gate charge					nC
Q_{gs}	Gate-source charge	$V_{DD} = 15 \text{ V}, I_D = 48 \text{ A}$ $V_{GS} = 5 \text{ V}$	-	8.8 4.7 2.2	-	nC
Q_{gd}	Gate-drain charge					nC
Q_{gs1}	Pre V_{th} gate-to-source charge	$V_{DD} = 15 \text{ V}, I_D = 48 \text{ A}$ $V_{GS} = 5 \text{ V}$	-	2.2	-	nC
Q_{gs2}	Post V_{th} gate-to-source charge			2.5	-	nC
R_G	Gate input resistance	$f = 1 \text{ MHz}$ gate bias Bias = 0 test signal level = 20 mV open drain	-	1.1	-	Ω

Table 6. Switching on/off (resistive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	$V_{DD}=10\text{ V}$, $I_D=24\text{ A}$, $R_G=4.7\text{ }\Omega$, $V_{GS}=10\text{ V}$	-	6 33	-	ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	$V_{DD}=10\text{ V}$, $I_D=24\text{ A}$, $R_G=4.7\text{ }\Omega$, $V_{GS}=10\text{ V}$	-	19 4.2	-	ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}	Source-drain current Source-drain current (pulsed) ⁽¹⁾		-		48 192	A A
V_{SD}	Forward on voltage	$I_{SD}=24\text{ A}$, $V_{GS}=0$	-		1.1	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=48\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}$, $V_{DD}=20\text{ V}$,	-	25 18.5 1.5		ns nC A

1. Pulsed: pulse duration = 300μs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

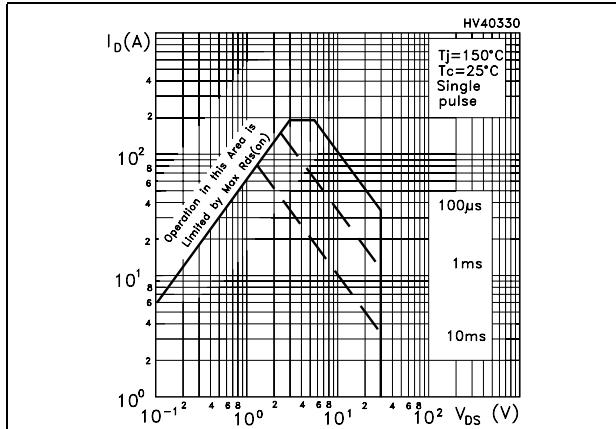


Figure 3. Thermal impedance

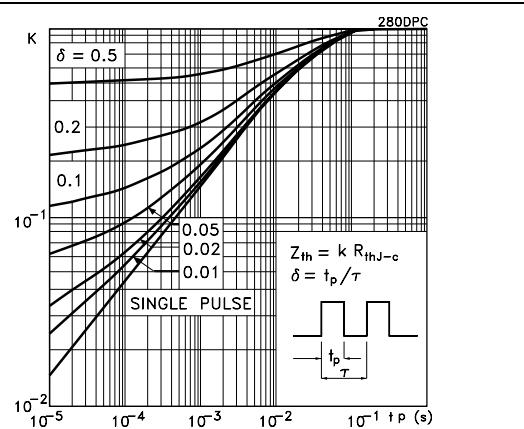


Figure 4. Output characteristics

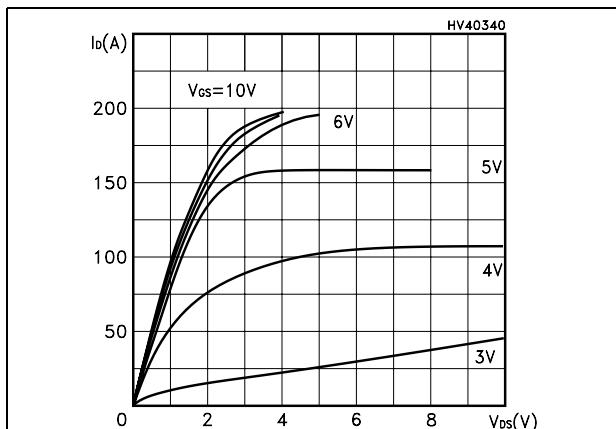


Figure 5. Transfer characteristics

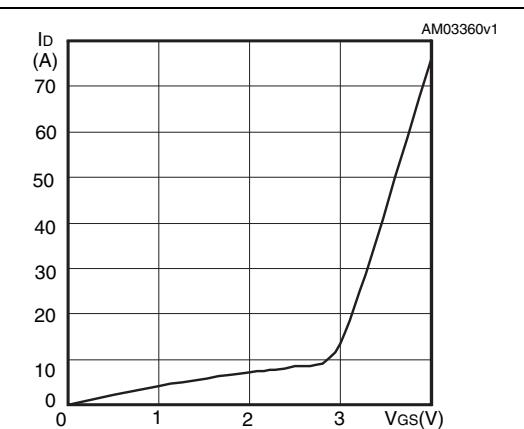
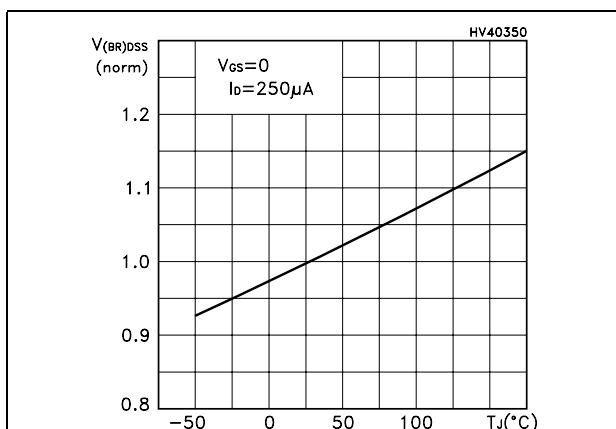
Figure 6. Normalized B_{VDSS} vs temperature

Figure 7. Static drain-source on resistance

