STD5N95K5, STF5N95K5, STP5N95K5, STU5N95K5

N-channel 950 V, 2 Ω typ., 3.5 A MDmesh™ K5 Power MOSFETs in DPAK, TO-220FP, TO-220 and IPAK

Datasheet - production data

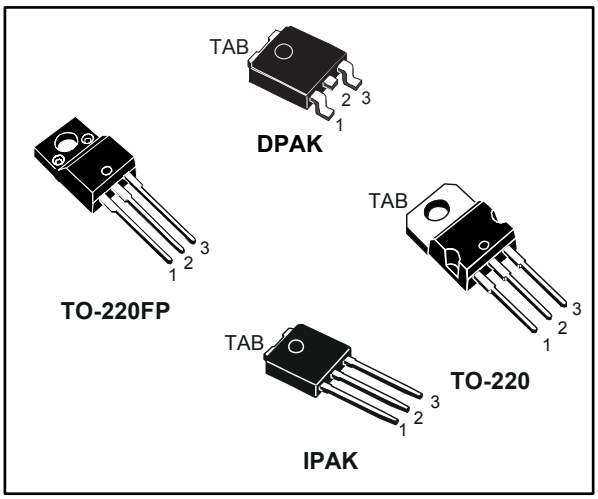
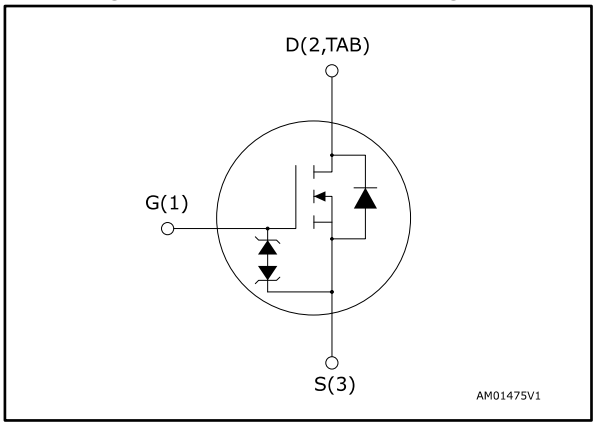


Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{tot}
STD5N95K5	950 V	2.5 Ω	3.5 A	70 W
STF5N95K5				25 W
STP5N95K5				70 W
STU5N95K5				70 W

- Industry's lowest $R_{DS(on)}$ x area
- Industry's best FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

These very high voltage N-channel Power MOSFETs are designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1: Device summary

Order code	Marking	Package	Packing
STD5N95K5	5N95K5	DPAK	Tape and reel
STF5N95K5		TO-220FP	Tube
STP5N95K5		TO-220	
STU5N95K5		IPAK	

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value		Unit
		DPAK, TO-220, IPAK	TO-220FP	
V_{GS}	Gate-source voltage	±30		V
I_D	Drain current (continuous) at T_C = 25 °C	3.5	3.5 (1)	A
I_D	Drain current (continuous) at T_C = 100 °C	2.2	2.2 (1)	A
I_{DM} (2)	Drain current pulsed	14		A
P_{TOT}	Total dissipation at T_C = 25 °C	70	25	W
dv/dt (3)	Peak diode recovery voltage slope	4.5		V/ns
dv/dt (4)	MOSFET dv/dt ruggedness	50		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s; T_C=25 °C)		2500	V
T_j	Operating junction temperature range	-55 to 150		°C
T_{stg}	Storage temperature range			

Notes:

(1)Limited by maximum junction temperature.

(2)Pulse width limited by safe operating area.

(3)I_{SD} ≤ 3.5 A, di/dt ≤ 100 A/µs, V_{DS} (peak) ≤ $V_{(BR)DSS}$

(4)V_{DS} ≤ 640 V

Table 3: Thermal data

Symbol	Parameter	Value				Unit
		DPAK	TO-220FP	TO-220	IPAK	
$R_{thj-case}$	Thermal resistance junction-case	1.47	5	1.47		°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient		62.5		100	°C/W
$R_{thj-pcb}$ (1)	Thermal resistance junction-pcb	50				°C/W

Notes:

(1)When mounted on 1 inch² FR-4, 2 Oz copper board

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	1	A
E_{AS}	Single pulse avalanche energy (starting Tj = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	70	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified

Table 5: On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	950			V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 950 V, V_{GS} = 0 V			1	µA
		V_{DS} = 950 V, V_{GS} = 0 V T_C = 125 °C(1)			50	µA
I_{GSS}	Gate body leakage current	V_{GS} = ±20 V, V_{DS} = 0 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 1.5 A		2	2.5	Ω

Notes:

(1)Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	220	-	pF
C_{oss}	Output capacitance		-	17	-	pF
C_{rss}	Reverse transfer capacitance		-	1	-	pF
$C_{o(tr)}$(1)	Equivalent capacitance time related	V_{GS} = 0 V, V_{DS} = 0 to 760 V	-	30	-	pF
$C_{o(er)}$(2)	Equivalent capacitance energy related		-	11	-	pF
R_g	Intrinsic gate resistance	f = 1 MHz open drain	-	17	-	Ω
Q_g	Total gate charge	V_{DD} = 760 V, I_D = 3.5 A V_{GS}= 10 V	-	12.5	-	nC
Q_{gs}	Gate-source charge		-	2	-	nC
Q_{gd}	Gate-drain charge		-	10	-	nC

Notes:

(1)$C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

(2)$C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD}= 475 V, I_D = 1.75 A, R_G = 4.7 Ω V_{GS} = 10 V	-	12	-	ns
t_r	Rise time		-	16	-	ns
$t_{d(off)}$	Turn-off delay time		-	32	-	ns
t_f	Fall time		-	25	-	ns

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		3.5	A
I_{SDM}	Source-drain current (pulsed)		-		14	A
V_{SD}(1)	Forward on voltage	I_{SD} = 3.5 A, V_{GS} = 0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 3.5 A, di/dt = 100 A/µs, V_{DD} = 60 V	-	330		ns
Q_{rr}	Reverse recovery charge		-	2.2		µC
I_{RRM}	Reverse recovery current		-	13		A
t_{rr}	Reverse recovery time	I_{SD} = 3.5 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_j = 150 °C	-	525		ns
Q_{rr}	Reverse recovery charge		-	3.2		µC
I_{RRM}	Reverse recovery current		-	12		A

Notes:

(1)Pulsed: pulse duration = 300 µs, duty cycle 1.5%

Table 9: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	I_{GS}= ± 1 mA, I_D= 0 A	30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection,thus eliminating the need for additional external componentry.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area for DPAK and IPAK

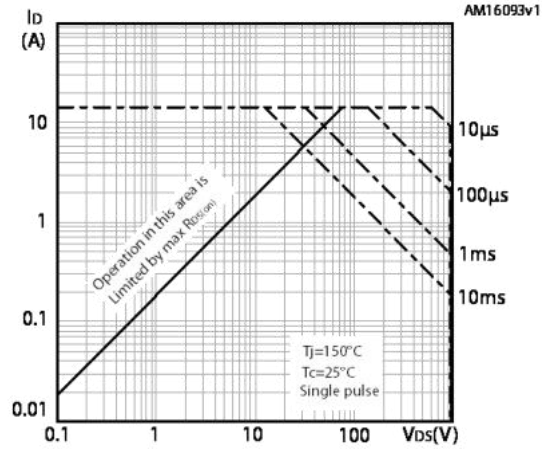


Figure 3: Thermal impedance for DPAK and IPAK

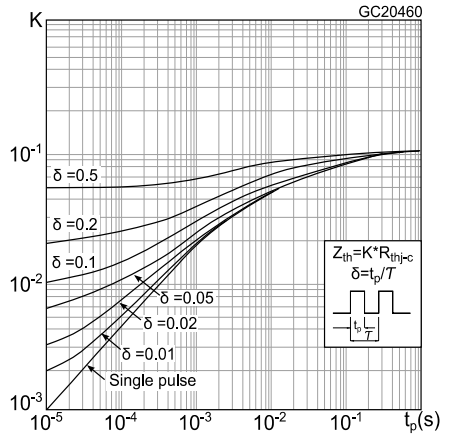


Figure 4: Safe operating area for TO-220FP

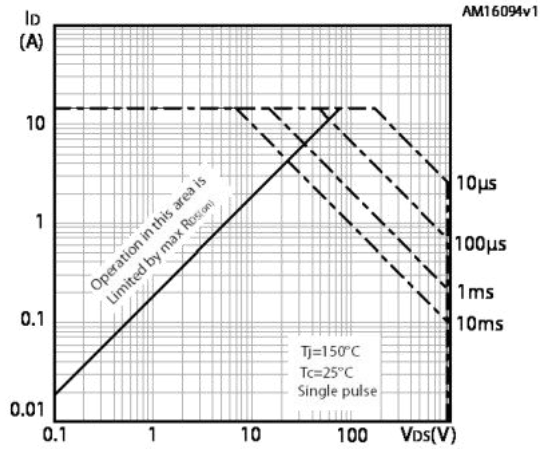


Figure 5: Thermal impedance for TO-220FP

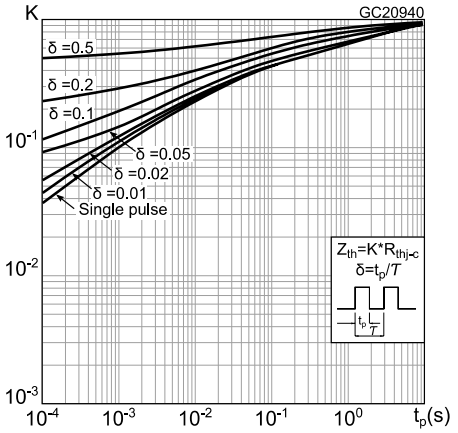


Figure 6: Safe operating area for TO-220

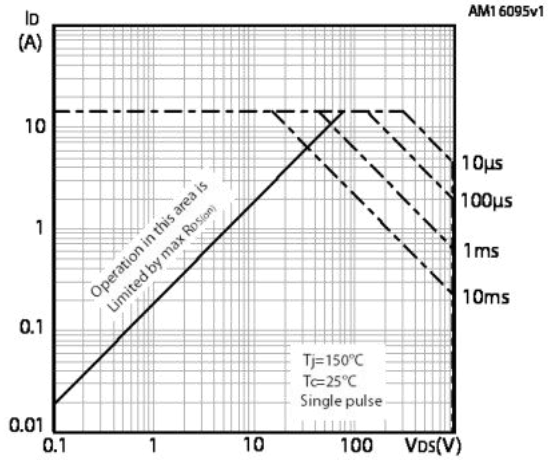


Figure 7: Thermal impedance for TO-220