STB5N52K3, STD5N52K3, STF5N52K3 STP5N52K3, STU5N52K3

N-channel 525 V, 1.2 Ω, 4.4 A SuperMESH3™ Power MOSFET
D²PAK, DPAK, TO-220FP, TO-220, IPAK

Features

Order codes	V_{DSS}	$R_{DS(on)}$ max	I_D	P_w
STB5N52K3	525 V	< 1.5 Ω	4.4 A	70 W
STD5N52K3				70 W
STF5N52K3				25 W
STP5N52K3				70 W
STU5N52K3				70 W

- 100% avalanche tested
- Extremely high dv/dt capability
- Gate charge minimized
- Very low intrinsic capacitance
- Improved diode reverse recovery characteristics
- Zener-protected

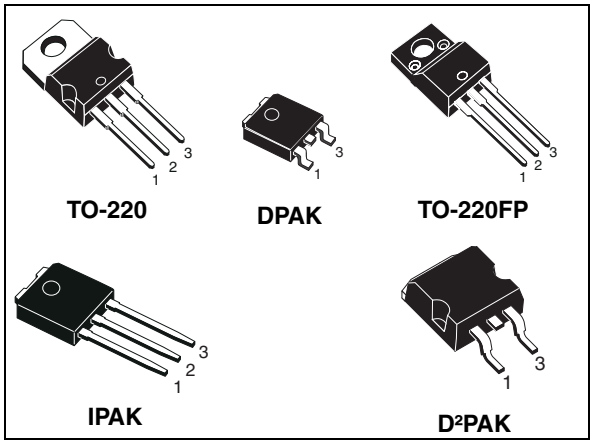
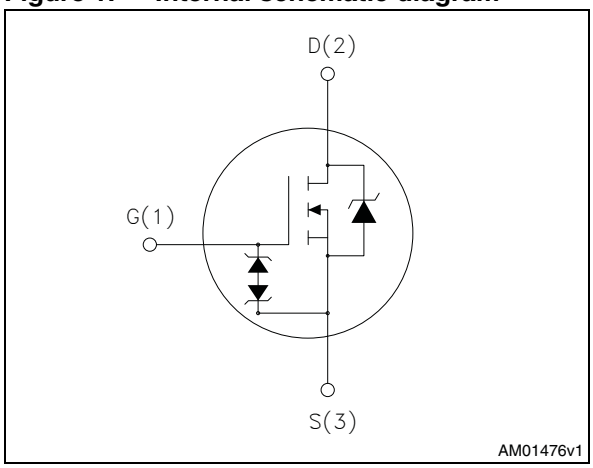


Figure 1. Internal schematic diagram



Application

Switching applications

Description

These devices are made using the SuperMESH3™ Power MOSFET technology that is obtained via improvements applied to STMicroelectronics' SuperMESH™ technology combined with a new optimized vertical structure. The resulting product has an extremely low on resistance, superior dynamic performance and high avalanche capability, making it especially suitable for the most demanding applications.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STB5N52K3	5N52K3	D²PAK	Tape and reel
STD5N52K3		DPAK	
STF5N52K3		TO-220FP	Tube
STP5N52K3		TO-220	
STU5N52K3		IPAK	

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value			Unit
		TO-220 D²PAK	DPAK IPAK	TO-220FP	
V_{DS}	Drain- source voltage	525			V
V_{GS}	Gate- source voltage	± 30			V
I_D	Drain current (continuous) at T_C = 25 °C	4.4		4.4(1)	A
I_D	Drain current (continuous) at T_C = 100 °C	2.77		2.77 (1)	A
I_{DM} (2)	Drain current (pulsed)	17.6		17.6(1)	A
P_{TOT}	Total dissipation at T_C = 25 °C	70		25	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max)	2.2			A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	100			mJ
dv/dt(3)	Peak diode recovery voltage slope	12			V/ns
V_{ISO}	Insulation withstand voltage (AC)			2500	V
T_J T_{stg}	Operating junction temperature Storage temperature	- 55 to 150			°C

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. $I_{SD} \leq$ 4.4 A, di/dt $\leq$ 100 A/µs,V_{DS} peak $\leq V_{(BR)DSS}$, V_{DD} = 80% $V_{(BR)DSS}$.

Table 3. Thermal data

Symbol	Parameter	Value					Unit
		TO-220	D²PAK	TO-220FP	IPAK	DPAK	
$R_{thj-case}$	Thermal resistance junction-case max.	1.79		5	1.79		°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5			100		°C/W
$R_{thj-pcb}$	Thermal resistance junction-pcb max.		30			50	°C/W
T_J	Maximum lead temperature for soldering purpose	300		300			°C/W

2 Electrical characteristics

(Tcase =25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	525			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating V_{DS} = Max rating, T_C=125 °C			1 50	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V; V_{DS}=0			10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 50 µA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 2.2 A		1.2	1.5	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0	-	545 45 8	-	pF pF pF
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{DS} = 0 to 420 V, V_{GS} = 0	-	33	-	pF
R_g	Gate input resistance	f=1 MHz open drain	-	4.7	-	Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 420 V, I_D = 4.4 A, V_{GS} = 10 V	-	17 3 10	-	nC nC nC

1. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 420 V, I_D = 4.4 A, R_G = 4.7 Ω, V_{GS} = 10 V	-	9	-	ns
t_r	Rise time			11		ns
$t_{d(off)}$	Turn-off-delay time			29		ns
t_f	Fall time			16		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current		-		4.4	A
I_{SDM} (1)	Source-drain current (pulsed)				17.6	A
V_{SD} (2)	Forward on voltage	I_{SD} = 4.4 A, V_{GS} = 0	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 4.4 A, di/dt = 100 A/µs V_{DD}= 60 V	-	210		ns
Q_{rr}	Reverse recovery charge			1.3		µC
I_{RRM}	Reverse recovery current			12		A
t_{rr}	Reverse recovery time	I_{SD} = 4.4 A, di/dt = 100 A/µs V_{DD}= 60 V T_J = 150 °C	-	240		ns
Q_{rr}	Reverse recovery charge			1.6		µC
I_{RRM}	Reverse recovery current			13		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-source breakdown voltage	Igs=± 1 mA (open drain)	30	-		V

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area TO-220, D²PAK

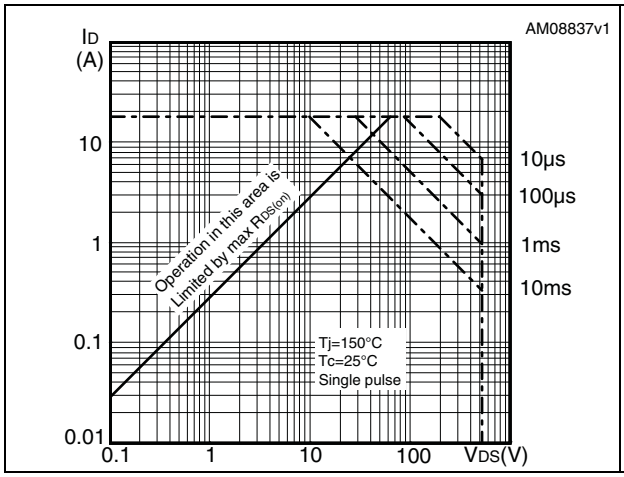


Figure 3. Thermal impedance TO-220, D²PAK

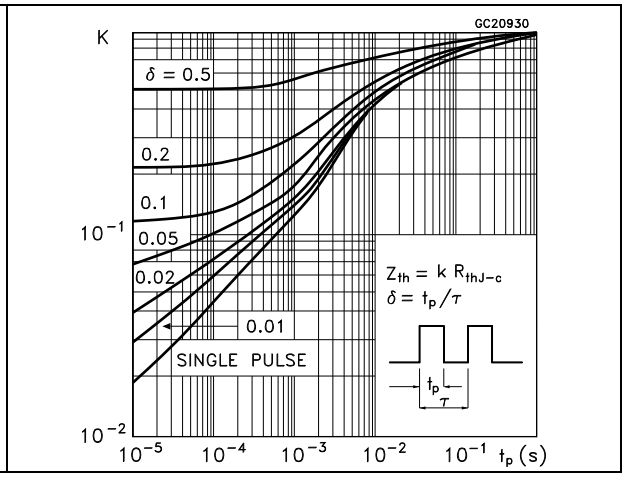


Figure 4. Safe operating area TO-220FP

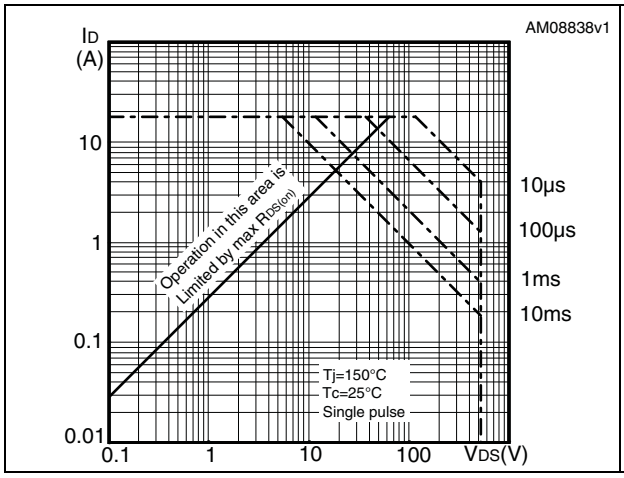


Figure 5. Thermal impedance TO-220FP

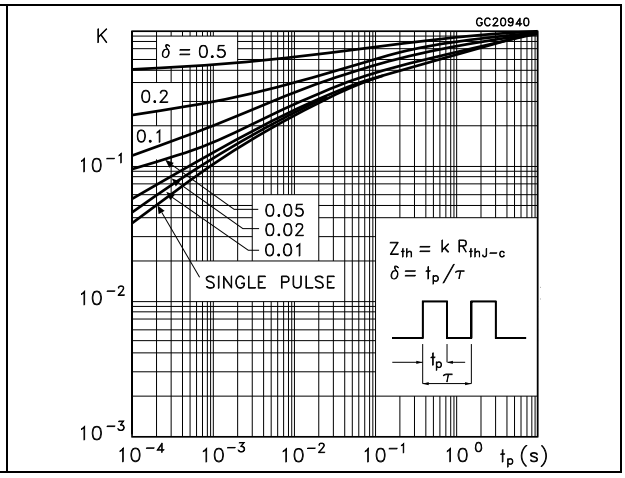


Figure 6. Safe operating area DPAK, IPAK

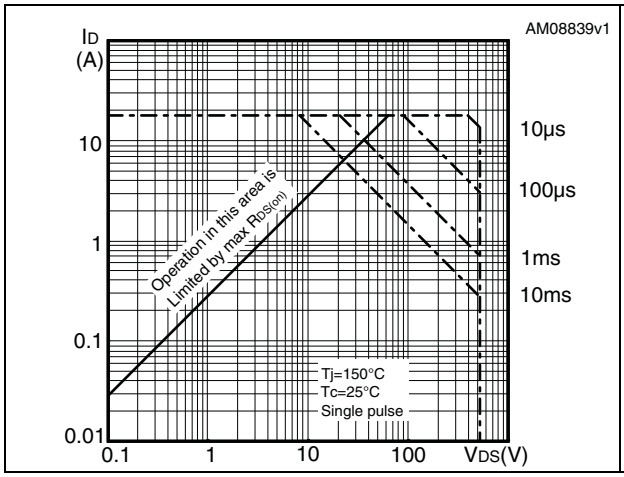


Figure 7. Thermal impedance DPAK, IPAK