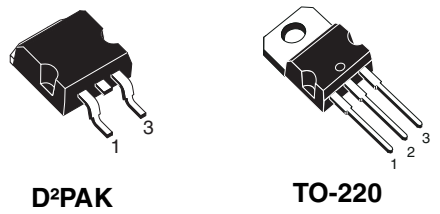
STB50NF25
STP50NF25

N-channel 250V - 0.055Ω - 45A - D^2PAK - TO-220
low gate charge STripFET™ Power MOSFET

Features

Type	V_{DSS}	$R_{DS(on)}$ Max	I_D	P_W
STP50NF25	250 V	<0.069 Ω	45 A	160 W
STB50NF25	250 V	<0.069 Ω	45 A	160 W

- 100% avalanche tested
- Gate charge minimized
- Low intrinsic capacitances



Application

Switching applications

Description

This Power MOSFET series realized with STMicroelectronics unique STripFET™ process has specifically been designed to minimize on-resistance and gate charge. It is therefore suitable as primary side switch allowing high efficiencies.

Figure 1. Internal schematic diagram

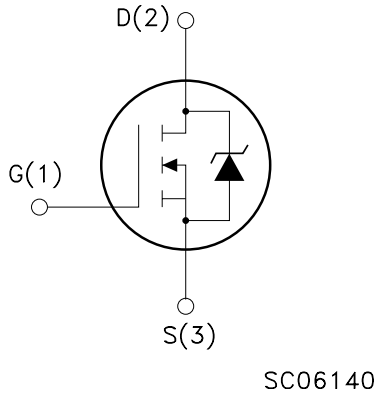


Table 1. Device summary

Order codes	Marking	Package	Packaging
STP50NF25	50NF25	TO-220	Tube
STB50NF25	50NF25	D²PAK	Tape & reel

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	250	V
V_{GS}	Gate-source voltage	±20	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	45	A
I_D (1)	Drain current (continuous) at T_C = 100 °C	28	A
I_{DM} (2)	Drain current (pulsed)	180	A
P_{TOT}	Total dissipation at T_C = 25 °C	160	W
	Derating factor	1.28	W/°C
dv/dt (3)	Peak diode recovery voltage slope	10	V/ns
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 150	°C

1. Value limited by wire bonding
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 45$ A, di/dt ≤ 200 A/µs, V_{DD} = 80% $V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
Rthj-case	Thermal resistance junction-case max	0.78	°C/W
Rthj-amb	Thermal resistance junction-amb max	62.5	°C/W
T_l	Maximum lead temperature for soldering purpose	300	°C

Table 4. Avalanche data

Symbol	Parameter	Value	Unit
I_{AR} (1)	Avalanche current, repetitive or not-repetitive	32	A
E_{AS} (2)	Single pulse avalanche energy	160	mJ

1. Pulse width limited by Tjmax
2. Starting T_J= 25 °C, $I_D = I_{AR}$, V_{DD} = 50 V

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS}= 0	250			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating, V_{DS} = Max rating @125 °C			1 10	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS}= 10 V, I_D= 22 A		0.055	0.069	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} =10 V, I_D = 22 A		20		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} =25 V, f=1 MHz, V_{GS}=0		2670 465 70.5		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD}=200 V, I_D = 45 A V_{GS} =10 V		68.2 12.2 33.4		nC nC nC
R_G	Gate input resistance	f=1 MHz Gate Bias, Bias=0 Test signal level=20 mV open drain		1.1		Ω

1. Pulsed: pulse duration=300µs, duty cycle 1.5%

Table 7. Switching times

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	V_{DD} = 125 V, I_D = 22 A, R_G = 4.7 Ω, V_{GS} = 10 V		45 26		ns ns
$t_{d(off)}$ t_f	Off-voltage rise time Fall time	V_{DD} = 125 V, I_D = 22 A, R_G = 4.7 Ω, V_{GS} = 10 V		63 20		ns ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
I_{SD} I_{SDM}	Source-drain current Source-drain current (pulsed)				45 180	A A
V_{SD}	Forward on voltage	I_{SD} = 45 A, V_{GS} = 0			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD}= 45 A, di/dt = 100 A/µs, V_{DD} = 60 V		198 1.5 15		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 45 A, di/dt = 100 A/µs, V_{DD} = 60 V, Tj = 150 °C		256 2.2 17		ns µC A

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

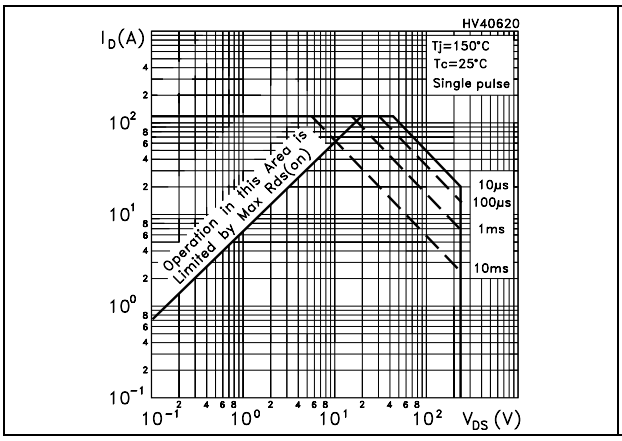


Figure 3. Thermal impedance

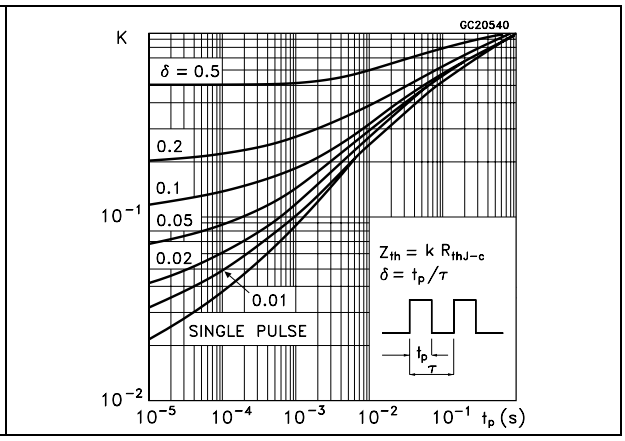


Figure 4. Output characteristics

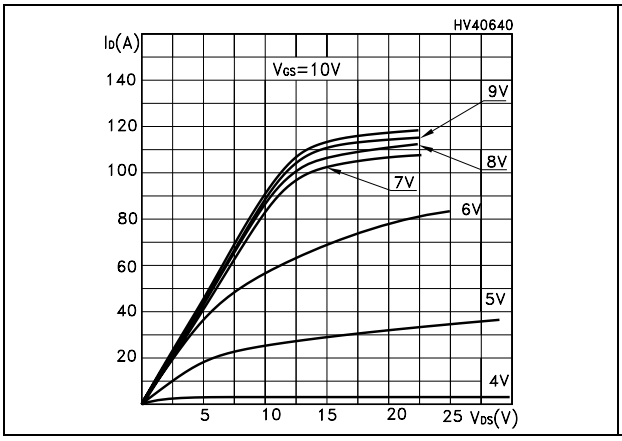


Figure 5. Transfer characteristics

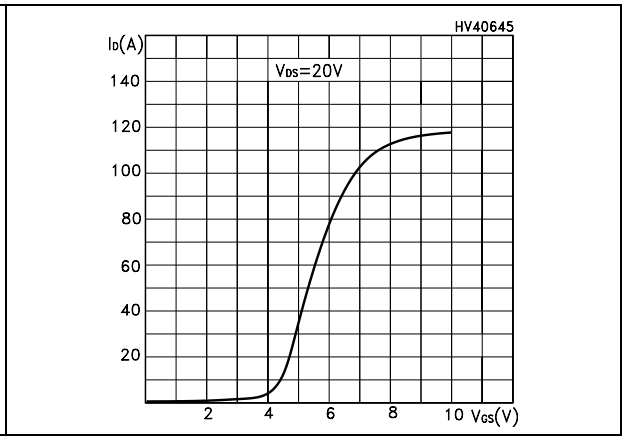


Figure 6. Normalized B_{VDSS} vs temperature

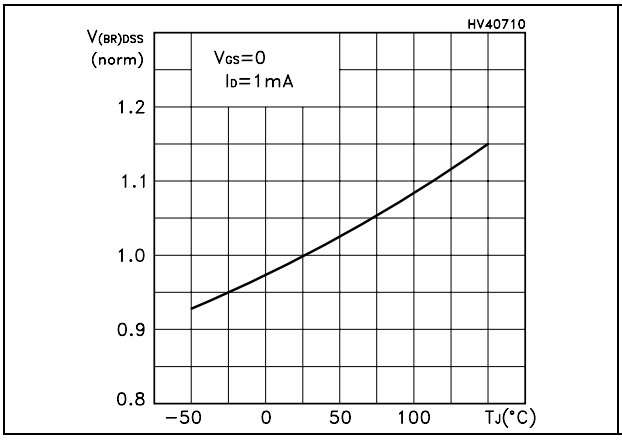


Figure 7. Static drain-source on resistance