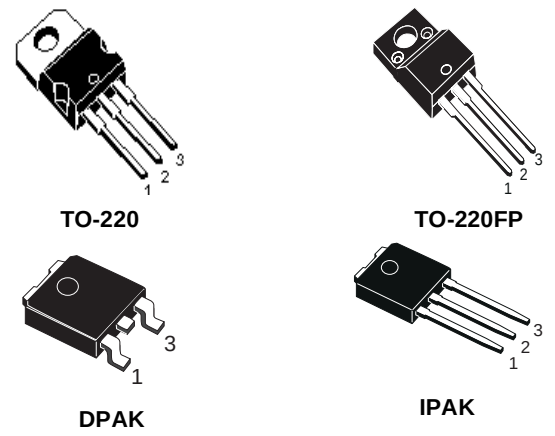
STP4NK50Z - STP4NK50ZFP
STD4NK50Z - STD4NK50Z-1

N-CHANNEL 500V - 2.4Ω - 3A TO-220/TO-220FP/DPAK/IPAK
Zener-Protected SuperMESH™Power MOSFET

TYPE	V_{DSS}	$R_{DS(on)}$	I_D	Pw
STP4NK50Z	500 V	< 2.7 Ω	3 A	45 W
STP4NK50ZFP	500 V	< 2.7 Ω	3 A	20 W
STD4NK50Z	500 V	< 2.7 Ω	3 A	45 W
STD4NK50Z-1	500 V	< 2.7 Ω	3 A	45 W

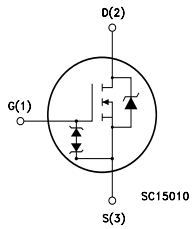
- TYPICAL R_{DS}(on) = 2.3 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- GATE CHARGE MINIMIZED
- VERY LOW INTRINSIC CAPACITANCES
- VERY GOOD MANUFACTURING REPEATIBILITY



DESCRIPTION

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

INTERNAL SCHEMATIC DIAGRAM



APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- IDEAL FOR OFF-LINE POWER SUPPLIES, ADAPTORS AND PFC
- LIGHTING

ORDERING INFORMATION

SALES TYPE	MARKING	PACKAGE	PACKAGING
STP4NK50Z	P4NK50Z	TO-220	TUBE
STP4NK50ZFP	P4NK50ZFP	TO-220FP	TUBE
STD4NK50ZT4	D4NK50Z	DPAK	TAPE & REEL
STD4NK50Z-1	D4NK50Z	IPAK	TUBE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value			Unit
		STP4NK50Z	STP4NK50ZFP	STD4NK50Z STD4NK50Z-1	
V_{DS}	Drain-source Voltage (V_{GS} = 0)	500			V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	500			V
V_{GS}	Gate- source Voltage	± 30			V
I_D	Drain Current (continuous) at T_C = 25°C	3	3 (*)	3 (*)	A
I_D	Drain Current (continuous) at T_C = 100°C	1.9	1.9 (*)	1.9 (*)	A
I_{DM} (•)	Drain Current (pulsed)	12	12 (*)	12 (*)	A
P_{TOT}	Total Dissipation at T_C = 25°C	45	20	45	W
	Derating Factor	0.36	0.16	0.36	W/°C
$V_{ESD(G-S)}$	Gate source ESD(HBM-C=100pF, R=1.5KΩ)	2800			V
dv/dt (1)	Peak Diode Recovery voltage slope	4.5			V/ns
V_{ISO}	Insulation Withstand Voltage (DC)	-	2500	-	V
T_j T_{stg}	Operating Junction Temperature Storage Temperature	-55 to 150			°C

(●) Pulse width limited by safe operating area
(1) I_{SD} ≤3 A, di/dt ≤200A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_j ≤ $T_{JMAX.}$
(*) Limited only by maximum temperature allowed

THERMAL DATA

		TO-220	TO-220FP	DPAK IPAK	
Rthj-case	Thermal Resistance Junction-case (Max)	2.78	6.25	2.78	°C/W
Rthj-amb	Thermal Resistance Junction-ambient (Max)	62.5		100	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose	300			°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	3	A
E_{AS}	Single Pulse Avalanche Energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	120	mJ

GATE-SOURCE ZENER DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-Source Breakdown Voltage	Igs=± 1mA (Open Drain)	30			V

PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

ELECTRICAL CHARACTERISTICS (T_{CASE} =25°C UNLESS OTHERWISE SPECIFIED)

ON/OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 1 mA, V_{GS} = 0	500			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating, T_C = 125 °C			1 50	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 20V			±10	µA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 50µA	3	3.75	4.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10V, I_D = 1.5 A		2.3	2.7	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	V_{DS} = 15 V, I_D = 1.5 A		1.5		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		310 49 10		pF pF pF
$C_{oss\ eq.}$ (3)	Equivalent Output Capacitance	V_{GS} = 0V, V_{DS} = 0V to 400V		33		pF

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	V_{DD} = 250 V, I_D = 1.5 A R_G = 4.7Ω V_{GS} = 10 V (Resistive Load see, Figure 3)		10 7		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD} = 400 V, I_D = 3 A, V_{GS} = 10 V		12 3 7		nC nC nC

SWITCHING OFF

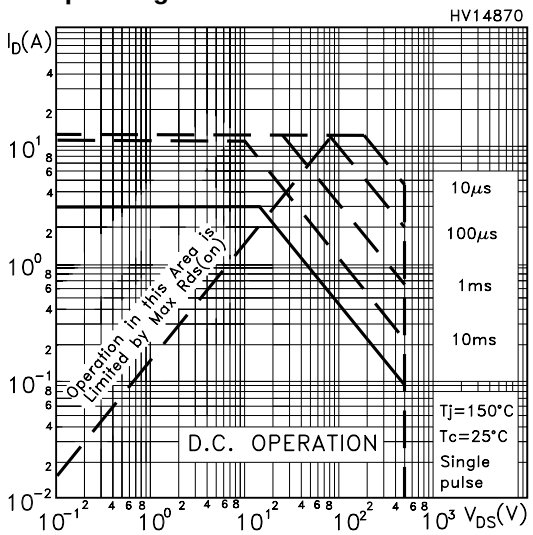
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	V_{DD} = 250 V, I_D = 1.5 A R_G = 4.7Ω V_{GS} = 10 V (Resistive Load see, Figure 3)		21 11		ns ns
$t_{r(Voff)}$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	V_{DD} = 400V, I_D = 3 A, R_G = 4.7Ω, V_{GS} = 10V (Inductive Load see, Figure 5)		10 10 17		ns ns ns

SOURCE DRAIN DIODE

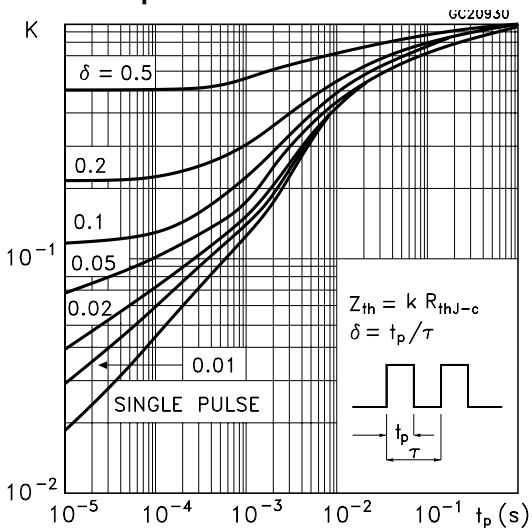
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (2)	Source-drain Current Source-drain Current (pulsed)				3 12	A A
V_{SD} (1)	Forward On Voltage	I_{SD} = 3 A, V_{GS} = 0			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 3 A, di/dt = 100A/µs V_{DD} = 40 V, T_j = 150°C (see test circuit, Figure 5)		260 935 7.2		ns nC A

Note: 1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
2. Pulse width limited by safe operating area.
3. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

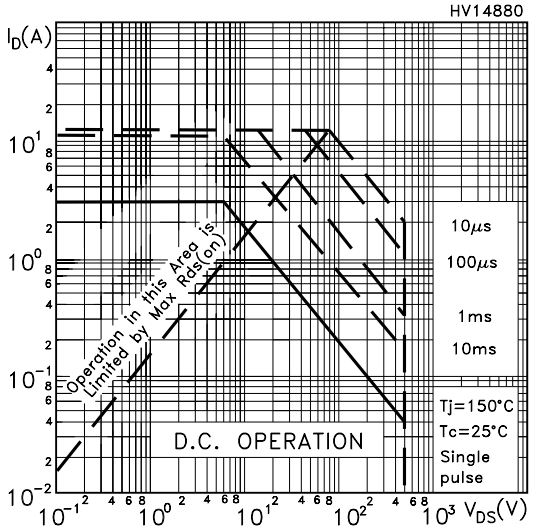
Safe Operating For TO-220



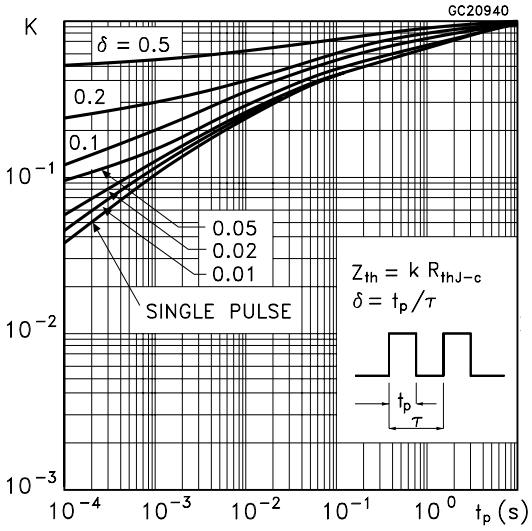
Thermal Impedance For TO-220



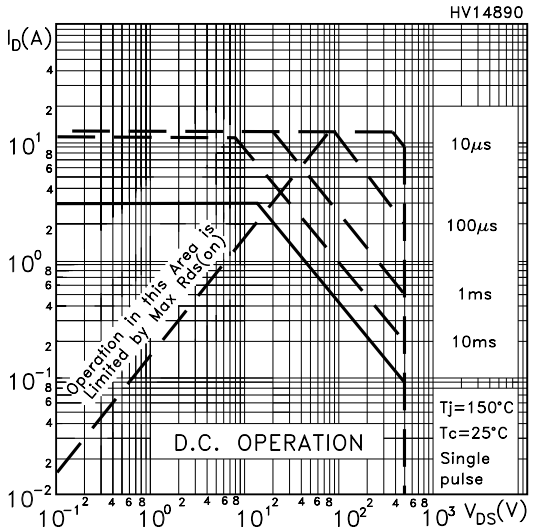
Safe Operating Area For TO-220FP



Thermal Impedance For TO-220FP



Safe Operating Area For DPAK/IPAK



Thermal Impedance For DPAK/IPAK