

STD4N80K5, STF4N80K5, STP4N80K5, STU4N80K5

N-channel 800 V, 2.1 Ω typ., 3 A MDmesh™ K5 Power MOSFETs
in DPAK, TO-220FP, TO-220 and IPAK packages

Datasheet - production data

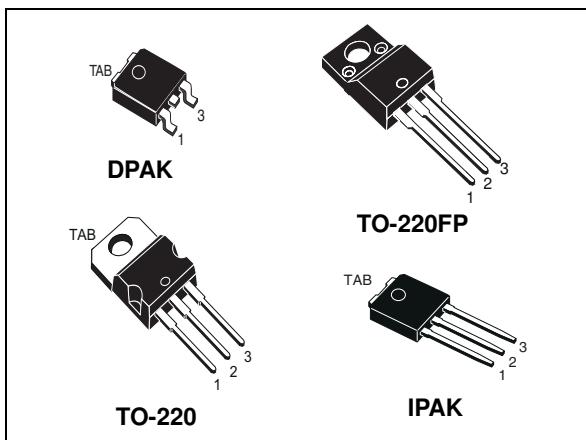
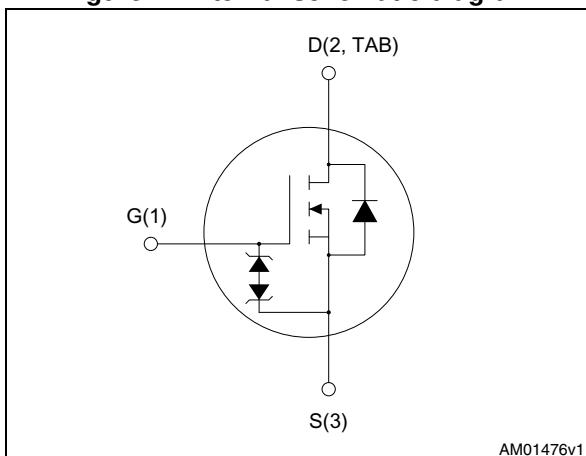


Figure 1. Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D	P _{TOT}
STD4N80K5	800 V	2.5 Ω	3 A	60 W
STF4N80K5				20 W
STP4N80K5				
STU4N80K5				60 W

- Industry's lowest R_{DS(on)} x area
- Industry's best figure of merit (FoM)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

These very high voltage N-channel Power MOSFETs are designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1. Device summary

Order code	Marking	Packages	Packaging
STD4N80K5	4N80K5	DPAK	Tape and reel
STF4N80K5		TO-220FP	Tube
STP4N80K5		TO-220	
STU4N80K5		IPAK	

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value			Unit
		DPAK, IPAK	TO-220FP	TO-220	
V_{DS}	Drain-source voltage	800			V
V_{GS}	Gate- source voltage	± 30			V
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$	3	3 ⁽¹⁾	3	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	1.7	1.7 ⁽¹⁾	1.7	A
$I_{DM}^{(2)}$	Drain current (pulsed)	12	12 ⁽¹⁾	12	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	60	20	60	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max)	1			A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50$ V)	74.5			mJ
$dv/dt^{(3)}$	Peak diode recovery voltage slope	4.5			V/ns
$dv/dt^{(4)}$	MOSFET dv/dt ruggedness	50			V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t = 1$ s, $T_C = 25^\circ\text{C}$)		2500		V
T_J	Operating junction temperature	-55 to 150			$^\circ\text{C}$
T_{stg}	Storage temperature				$^\circ\text{C}$

1. Limited by maximum junction temperature
2. Pulse width limited by safe operating area
3. $I_{SD} < 3$ A, $di/dt < 100$ A/ μs , $V_{DS(\text{peak})} \leq V_{(\text{BR})DSS}$
4. $V_{DS} \leq 640$ V

Table 3. Thermal data

Symbol	Parameter	Value			Unit
		DPAK, IPAK	TO-220FP	TO-220	
$R_{thj-case}$	Thermal resistance junction-case max	2.08	6.25	2.08	$^\circ\text{C/W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max		62.5		$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max	50			$^\circ\text{C/W}$

1. When mounted on 1inch² FR-4 board, 2 oz Cu

2 Electrical characteristics

(T_{case} =25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 1 mA, V _{GS} = 0	800			V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V _{DS} = 800 V			1	μA
		V _{DS} = 800 V, T _C =125 °C			50	μA
I _{GSS}	Gate-body leakage current (V _{DS} = 0)	V _{GS} = ± 20 V			±10	μA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 100 μA	3	4	5	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 1.5 A		2.1	2.5	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 100 V, f = 1 MHz, V _{GS} = 0	-	175	-	pF
C _{oss}	Output capacitance		-	18	-	pF
C _{rss}	Reverse transfer capacitance		-	0.5	-	pF
C _{o(tr)⁽¹⁾}	Equivalent capacitance time related	V _{DS} = 0 to 640 V, V _{GS} = 0	-	26	-	pF
C _{o(er)⁽²⁾}	Equivalent capacitance energy related	V _{DS} = 0 to 640 V, V _{GS} = 0	-	11	-	pF
R _g	Gate input resistance	f=1 MHz, I _D = 0	-	15	-	Ω
Q _g	Total gate charge	V _{DD} = 640 V, I _D = 3 A, V _{GS} = 10 V	-	10.5	-	nC
Q _{gs}	Gate-source charge		-	2	-	nC
Q _{gd}	Gate-drain charge		-	7.5	-	nC

1. Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
2. Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 400 \text{ V}, I_D = 1.5 \text{ A}, R_G = 4.7 \Omega, V_{GS} = 10 \text{ V}$	-	16.5	-	ns
t_r	Rise time		-	15	-	ns
$t_{d(off)}$	Turn-off-delay time		-	36	-	ns
t_f	Fall time		-	21	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		3	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				12	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 3 \text{ A}, V_{GS} = 0$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 3 \text{ A}, dI/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$ (see Figure 20)	-	242		ns
Q_{rr}	Reverse recovery charge		-	1.42		μC
I_{RRM}	Reverse recovery current		-	12		A
t_{rr}	Reverse recovery time	$I_{SD} = 3 \text{ A}, dI/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$ $T_J = 150^\circ\text{C}$	-	373		ns
Q_{rr}	Reverse recovery charge		-	1.98		μC
I_{RRM}	Reverse recovery current		-	10.5		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1 \text{ mA}, I_D = 0$	30	-	-	V

The built-in back-to-back Zener diodes have been specifically designed to enhance the ESD capability of the device. The Zener voltage is appropriate for efficient and cost-effective intervention to protect the device integrity. These integrated Zener diodes thus eliminate the need for external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for DPAK and IPAK

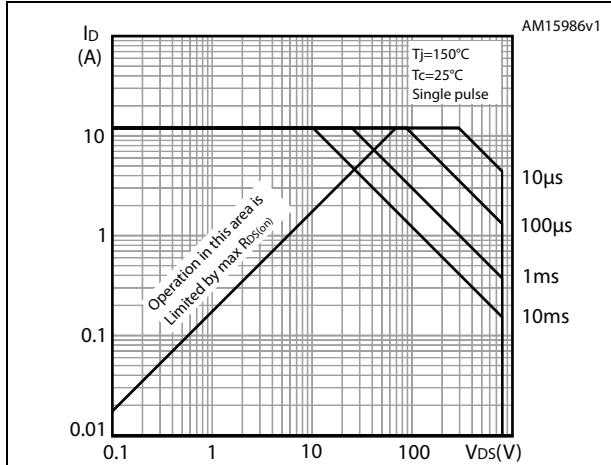


Figure 3. Thermal impedance for DPAK and IPAK

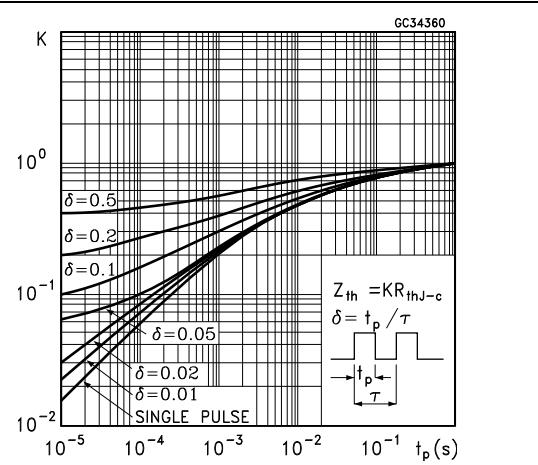


Figure 4. Safe operating area for TO-220FP

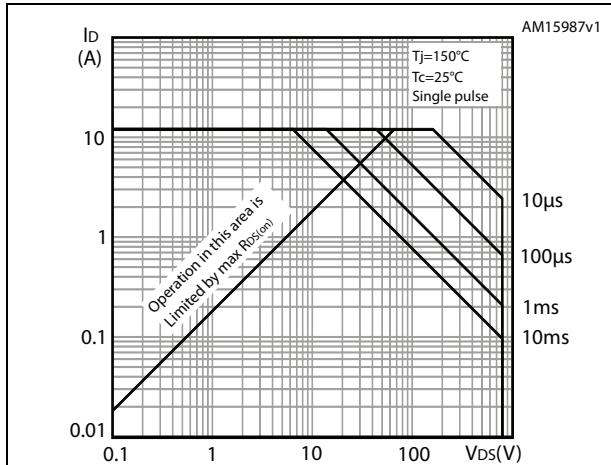


Figure 5. Thermal impedance for TO-220FP

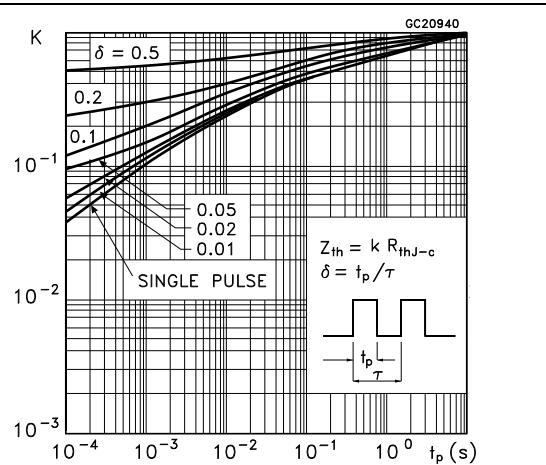


Figure 6. Safe operating area for TO-220

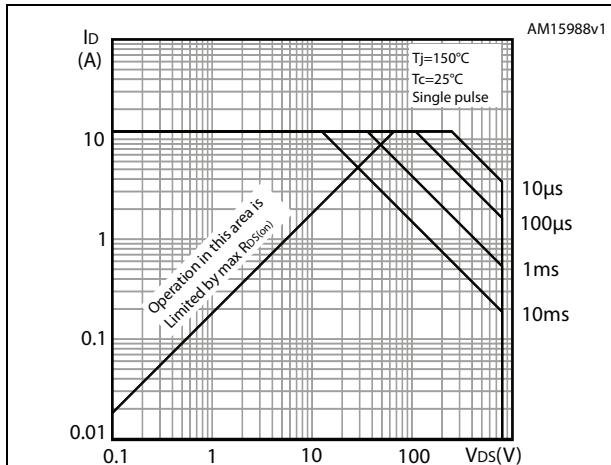


Figure 7. Thermal impedance for TO-220

