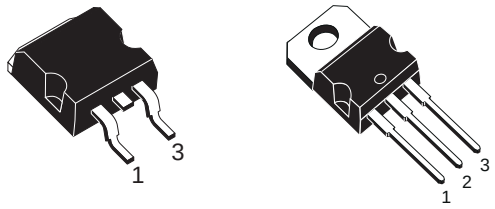
STP45NF06L
STB45NF06L

N-CHANNEL 60V - 0.022Ω - 38A TO-220 / D^2PAK
STripFET™ II POWER MOSFET

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STP45NF06L	60 V	< 0.028Ω	38 A
STB45NF06L	60 V	< 0.028Ω	38 A

- TYPICAL R_{DS}(on) = 0.022Ω
- EXCEPTIONAL dv/dt CAPABILITY
- LOGIC LEVEL GATE DRIVE

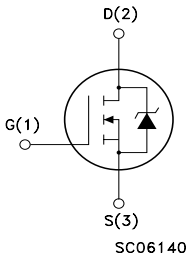


D^2PAK **TO-220**

DESCRIPTION

This Power Mosfet is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalance characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

INTERNAL SCHEMATIC DIAGRAM



APPLICATIONS

- HIGH-EFFICIENCY DC-DC CONVERTERS
- SOLENOID AND RELAY DRIVERS
- MOTOR CONTROL, AUDIO AMPLIFIERS
- DC-DC & DC-AC CONVERTERS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	60	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	60	V
V_{GS}	Gate- source Voltage	±16	V
I_D	Drain Current (continuos) at T_C = 25°C	38	A
I_D	Drain Current (continuos) at T_C = 100°C	26	A
I_{DM} (●)	Drain Current (pulsed)	152	A
P_{TOT}	Total Dissipation at T_C = 25°C	80	W
	Derating Factor	0.53	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	7	V/ns
T_{stg}	Storage Temperature	–55 to 175	°C
T_j	Max. Operating Junction Temperature		

(●) Pulse width limited by safe operating area

(1) I_{SD} ≤38A, di/dt ≤300A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_j ≤ T_{JMAX}.

THERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	1.87	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	62.5	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose	300	°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	38	A
E_{AS}	Single Pulse Avalanche Energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	135	mJ

ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0	60			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating			1	µA
		V_{DS} = Max Rating, T_C = 125 °C			10	µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ±16V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250µA	1	1.7	2.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 5 V, I_D = 19 A		0.024	0.03	Ω
		V_{GS} = 10V, I_D = 19 A		0.022	0.028	

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	V_{DS} =15V , I_D=19 A		24		S
C_{iss}	Input Capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		1600		pF
C_{oss}	Output Capacitance			217		pF
C_{rss}	Reverse Transfer Capacitance			62		pF

ELECTRICAL CHARACTERISTICS (CONTINUED)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	V_{DD} = 30V, I_D = 19A		30		ns
t_r	Rise Time	R_G = 4.7Ω V_{GS} = 10V (see test circuit, Figure 3)		105		ns
Q_g	Total Gate Charge	V_{DD} = 48V, I_D = 38A,		23	31	nC
Q_{gs}	Gate-Source Charge	V_{GS} = 5V		7		nC
Q_{gd}	Gate-Drain Charge			10		nC

SWITCHING OFF

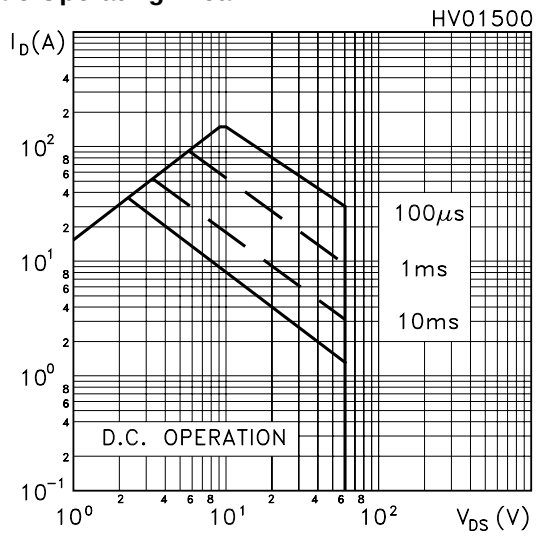
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off-Delay Time	V_{DD} = 30V, I_D = 19A,		65		ns
t_f	Fall Time	R_G = 4.7Ω, V_{GS} = 10V (see test circuit, Figure 3)		25		ns
$t_{d(off)}$	Off-voltage Rise Time	Vclamp =48V, I_D =38A R_G = 4.7Ω, V_{GS} = 10V		50		ns
t_f	Fall Time	(see test circuit, Figure 5)		55		ns
t_c	Cross-over Time			85		ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				38	A
I_{SDM} (2)	Source-drain Current (pulsed)				152	A
V_{SD} (1)	Forward On Voltage	I_{SD} = 38A, V_{GS} = 0			1.5	V
t_{rr}	Reverse Recovery Time	I_{SD} = 38A, di/dt = 100A/µs,		70		ns
Q_{rr}	Reverse Recovery Charge	V_{DD} = 100V, T_j = 150°C		110		nC
I_{RRM}	Reverse Recovery Current	(see test circuit, Figure 5)		4		A

Note: 1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

Safe Operating Area



Thermal Impedence