STD45N10F7, STI45N10F7, STP45N10F7

N-channel 100 V, 0.0145 Ω typ., 45 A, STripFET™ VII DeepGATE™ Power MOSFETs in DPAK, I^{2}PAK and TO-220 packages

Datasheet - production data

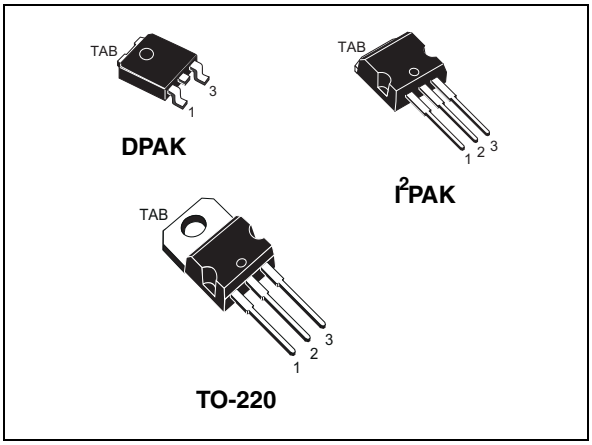
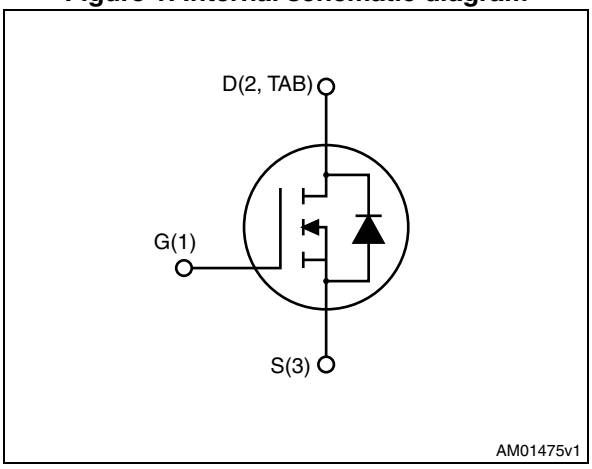


Figure 1. Internal schematic diagram



Features

Order codes	V_{DS}	$R_{DS(on)}$ max.(1)	I_D	P_{TOT}
STD45N10F7	100 V	0.018 Ω	45 A	60 W
STI45N10F7				
STP45N10F7				

1. @ V_{GS} = 10 V

- Ultra low on-resistance
- 100% avalanche tested

Applications

- Switching applications

Description

These devices utilize the 7th generation of design rules of ST's proprietary STripFET™ technology, with a new gate structure. The resulting Power MOSFET exhibits the lowest $R_{DS(on)}$ in all packages.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STD45N10F7	45N10F7	DPAK	Tape and reel
STI45N10F7		I^{2}PAK	Tube
STP45N10F7		TO-220	

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	100	V
V_{GS}	Gate-source voltage	20	V
I_D	Drain current (continuous) at T_C = 25 °C	45	A
I_D	Drain current (continuous) at T_C = 100 °C	32	A
I_{DM}(1)	Drain current (pulsed)	180	A
P_{TOT}	Total dissipation at T_c = 25 °C	60	W
T_J	Operating junction temperature	-55 to 175	°C
T_{stg}	Storage temperature		°C

1. Pulse width limited by safe operating area.

Table 3. Thermal resistance

Symbol	Parameter	Value		Unit
		DPAK	TO-220 I^2PAK	
$R_{thj-case}$	Thermal resistance junction-case	2.5	2.5	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient		62.5	°C/W
$R_{thj-pcb}$ (1)	Thermal resistance junction-pcb	31.2		°C/W

1. When mounted on FR-4 board of 1inch², 2oz Cu, t < 10 sec.

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage (V_{GS}= 0)	I_D = 1 mA	100		-	V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 100 V			10	µA
		V_{DS} = 100 V; T_C =125 °C			100	µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2.5		4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 22.5 A		0.0145	0.018	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 50 V, f =1 MHz, V_{GS} = 0	-	1640	-	pF
C_{oss}	Output capacitance		-	360	-	pF
C_{rss}	Reverse transfer capacitance		-	25	-	pF
Q_g	Total gate charge	V_{DD} = 50 V, I_D = 45 A V_{GS} = 10 V	-	25	-	nC
Q_{gs}	Gate-source charge		-	5.1	-	nC
Q_{gd}	Gate-drain charge		-	12.2	-	nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 50 V, I_D = 22.5 A, R_G = 4.7 Ω, V_{GS} = 10 V	-	15	-	ns
t_r	Rise time		-	17	-	ns
$t_{d(off)}$	Turn-off delay time		-	24	-	ns
t_f	Fall time		-	8	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		45	A
I_{SDM}(1)	Source-drain current (pulsed)		-		180	A
V_{SD}(2)	Forward on voltage	I_{SD} = 45 A, V_{GS} = 0	-		1.1	V
t_{rr}	Reverse recovery time	I_{SD} = 45 A, di/dt = 100 A/µs, V_{DD} = 80 V, T_j = 150 °C	-	53		ns
Q_{rr}	Reverse recovery charge		-	67		nC
I_{RRM}	Reverse recovery current		-	2.5		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration=300 µs, duty cycle 1.5%.