STB40N60M2, STP40N60M2, STW40N60M2

N-channel 600 V, 0.078 Ω typ., 34 A MDmesh II Plus™ low Q_g Power MOSFETs in D^2PAK, TO-220 and TO-247 packages

Datasheet — production data

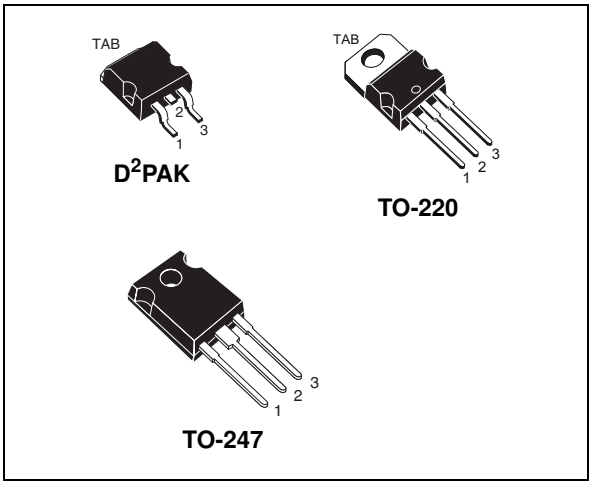
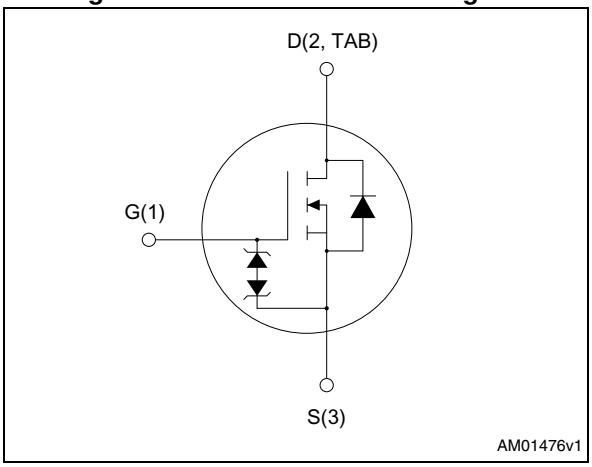


Figure 1. Internal schematic diagram



Features

Order codes	V_{DS} @ T_{Jmax}	$R_{DS(on)}$ max	I_D
STB40N60M2	650 V	0.088 Ω	34 A
STP40N60M2			
STW40N60M2			

- Extremely low gate charge
- Lower $R_{DS(on)}$ x area vs previous generation
- Low gate input resistance
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications
- LLC converters, resonant converters

Description

These devices are N-channel Power MOSFETs developed using a new generation of MDmesh™ technology: MDmesh II Plus™ low Q_g. These revolutionary Power MOSFETs associate a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. They are therefore suitable for the most demanding high efficiency converters.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STB40N60M2	40N60M2	D^2PAK	Tape and reel
STP40N60M2		TO-220	Tube
STW40N60M2		TO-247	

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at T_C = 25 °C	34	A
I_D	Drain current (continuous) at T_C = 100 °C	22	A
I_{DM}(1)	Drain current (pulsed)	136	A
P_{TOT}	Total dissipation at T_C = 25 °C	250	W
dv/dt (2)	Peak diode recovery voltage slope	15	V/ns
dv/dt(3)	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature	- 55 to 150	°C
T_j	Max. operating junction temperature		°C

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 34$ A, di/dt ≤ 400 A/μs; $V_{DS\ peak} < V_{(BR)DSS}$, V_{DD}=400 V.
3. $V_{DS} \leq 480$ V

Table 3. Thermal data

Symbol	Parameter	Value			Unit
		D^2PAK	TO-220	TO-247	
$R_{thj\text{-}case}$	Thermal resistance junction-case max	0.50			°C/W
$R_{thj\text{-}pcb}$	Thermal resistance junction-pcb max(1)	30			°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max		62.5	50	°C/W

1. When mounted on 1 inch² FR-4, 2 Oz copper board

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	6	A
E_{AS}	Single pulse avalanche energy (starting T_j=25°C, I_D= I_{AR}; V_{DD}=50 V)	500	mJ

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0, I_D = 1 mA	600			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0, V_{DS} = 600 V			1	µA
		V_{GS} = 0, V_{DS} = 600 V, T_C=125 °C			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0, V_{GS} = ± 25 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 17 A		0.078	0.088	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0	-	2500	-	pF
C_{oss}	Output capacitance		-	117	-	pF
C_{rss}	Reverse transfer capacitance		-	2.4	-	pF
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{DS} = 0 to 480 V, V_{GS} = 0	-	342	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D = 0	-	4.4	-	Ω
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 34 A, V_{GS} = 10 V	-	57	-	nC
Q_{gs}	Gate-source charge		-	10	-	nC
Q_{gd}	Gate-drain charge		-	25.5	-	nC

1. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 34 A, R_G = 4.7 Ω, V_{GS} = 10 V	-	20.5	-	ns
t_r	Rise time		-	13.5	-	ns
$t_{d(off)}$	Turn-off-delay time		-	96	-	ns
t_f	Fall time		-	11	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-	34		A
I_{SDM} (1)	Source-drain current (pulsed)		-	136		A
V_{SD} (2)	Forward on voltage	I_{SD} = 34 A, V_{GS} = 0	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 34 A, di/dt = 100 A/µs V_{DD} = 60 V (see	-	440		ns
Q_{rr}	Reverse recovery charge		-	8.2		µC
I_{RRM}	Reverse recovery current		-	37		A
t_{rr}	Reverse recovery time	I_{SD} = 34 A, di/dt = 100 A/µs V_{DD} = 60 V, T_j = 150 °C	-	568		ns
Q_{rr}	Reverse recovery charge		-	11.5		µC
I_{RRM}	Reverse recovery current		-	40.5		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for D²PAK and TO-220

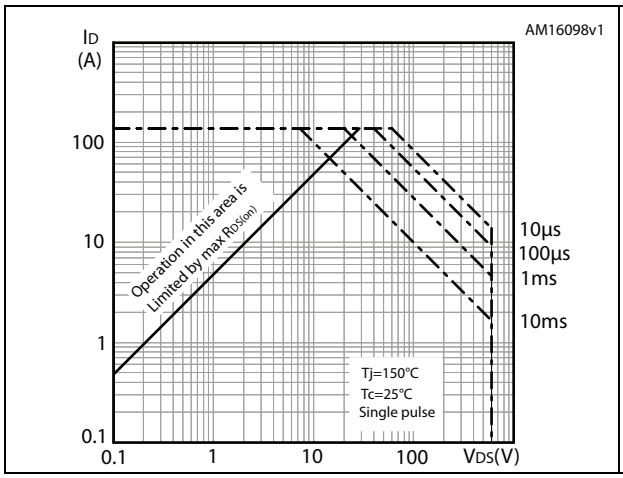


Figure 3. Thermal impedance D²PAK and TO-220

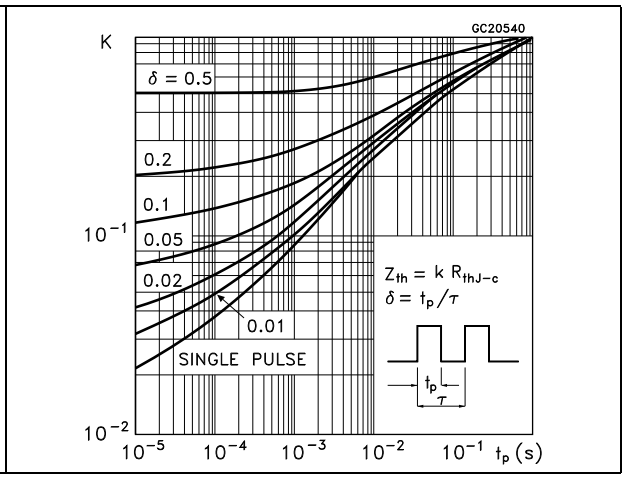


Figure 4. Safe operating area for TO-247

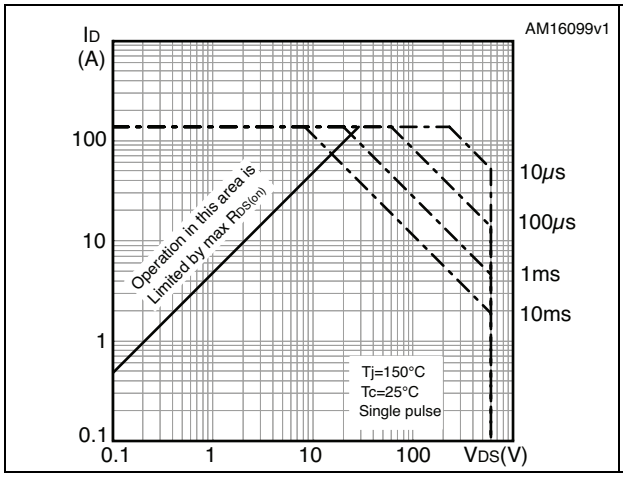


Figure 5. Thermal impedance for TO-247

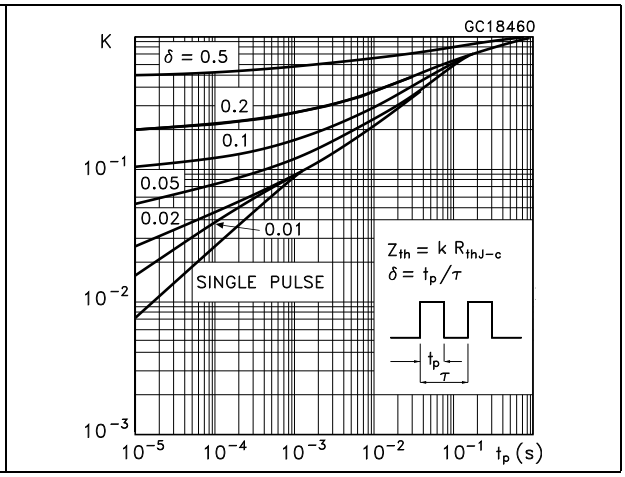


Figure 6. Output characteristics

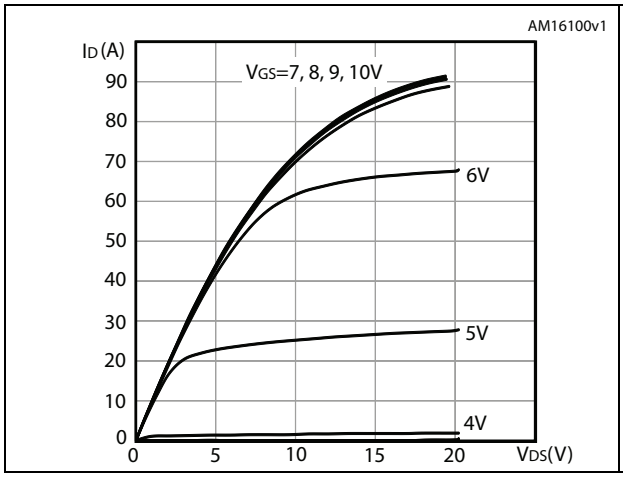


Figure 7. Transfer characteristics