# STFV3N150 , STFW3N150
# STP3N150, STW3N150

N-channel 1500 V, 6 Ω, 2.5 A, PowerMESH™ Power MOSFET
TO-220, TO-220FH, TO-247, TO-3PF

## Features

| Type | $V_{DSS}$ | $R_{DS(on)}$ max | $I_D$ | Pw |
|---|---|---|---|---|
| STFV3N150 | 1500 V | < 9 Ω | 2.5 A | 30 W |
| STFW3N150(1) | 1500 V | < 9 Ω | 2.5 A | 83 W |
| STP3N150 | 1500 V | < 9 Ω | 2.5 A | 140 W |
| STW3N150 | 1500 V | < 9 Ω | 2.5 A | 140 W |

1. All data which refers solely to the TO-3PF package is preliminary

- 100% avalanche tested
- Intrinsic capacitances and Qg minimized
- High speed switching
- Fully isolated TO-3PF and TO-220FH plastic packages
- Creepage distance path is 5.4 mm (typ.) for TO-3PF
- Creepage distance path is > 4 mm for TO-220FH

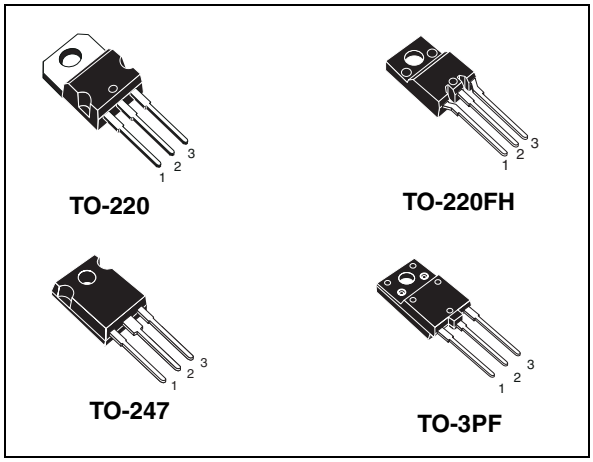
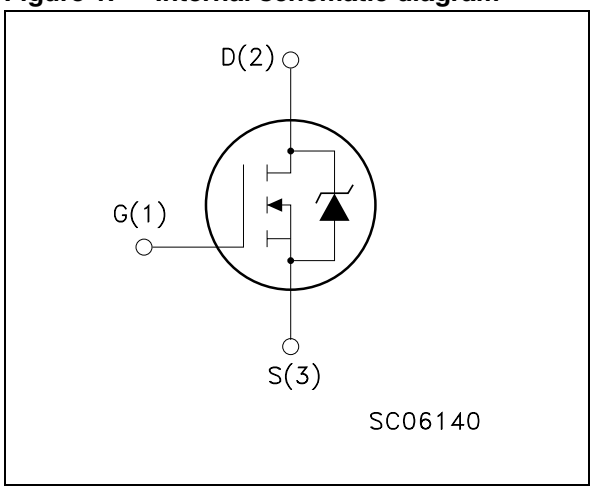



**Figure 1. Internal schematic diagram**




## Application

- Switching applications

## Description

Using the well consolidated high voltage MESH OVERLAY™ process, STMicroelectronics has designed an advanced family of very high voltage Power MOSFETs with outstanding performances. The strengthened layout coupled with the company's proprietary edge termination structure, gives the lowest $R_{DS(on)}$ per area, unrivalled gate charge and switching characteristics.

**Table 1. Device summary**

| Order codes | Marking | Package | Packaging |
|---|---|---|---|
| STFV3N150 | 3N150 | TO-220FH | Tube |
| STFW3N150 | 3N150 | TO-3PF | Tube |
| STP3N150 | 3N150 | TO-220 | Tube |
| STW3N150 | 3N150 | TO-247 | Tube |

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

| Symbol | Parameter | Value | | | Unit |
|---|---|---|---|---|---|
| | | TO-220,TO-247 | TO-220FH | TO-3PF | |
| $V_{DS}$ | Drain-source voltage ($V_{GS}$ = 0) | 1500 | | | V |
| $V_{GS}$ | Gate-source voltage | ± 30 | | | V |
| $I_D$ | Drain current (continuous) at $T_C$ = 25 °C | 2.5 | 2.5 (1) | 2.5(1) | A |
| $I_D$ | Drain current (continuous) at $T_C$ = 100 °C | 1.6 | 1.6 (1) | 1.6 (1) | A |
| $I_{DM}$ (2) | Drain current (pulsed) | 10 | 10 (1) | 10 (1) | A |
| $P_{TOT}$ | Total dissipation at $T_C$ = 25 °C | 140 | 30 | 83 | W |
| $V_{ISO}$ | Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s;$T_C$=25 °C) | | 2500 | TBD | V |
| | Derating factor | 1.12 | 0.24 | 0.67 | W/°C |
| $T_{stg}$ | Storage temperature | -50 to 150 | | | °C |
| $T_j$ | Max. operating junction temperature | 150 | | | °C |

1. Limited by maximum temperature allowed
2. Pulse width limited by safe operating area

**Table 3. Thermal data**

| Symbol | Parameter | TO-220 | TO-247 | TO-220FH | TO-3PF | Unit |
|---|---|---|---|---|---|---|
| $R_{thj\text{-}case}$ | Thermal resistance junction-case max | 0.89 | | 4.17 | 1.5 | °C/W |
| $R_{thj\text{-}amb}$ | Thermal resistance junction-ambient max | 62.5 | 50 | 62.5 | 50 | °C/W |
| $T_j$ | Maximum lead temperature for soldering purpose | 300 | | | | °C/W |

**Table 4. Avalanche characteristics**

| Symbol | Parameter | Max value | Unit |
|---|---|---|---|
| $I_{AR}$ | Avalanche current, repetitive or not-repetitive (pulse width limited by $T_j$ max) | 2.5 | A |
| $E_{AS}$ | Single pulse avalanche energy (starting $T_j$ = 25 °C, $I_D$ = $I_{AR}$, $V_{DD}$ = 50 V) | 450 | mJ |

# 2 Electrical characteristics

($T_{case}$ = 25 °C unless otherwise specified)

**Table 5. On /off states**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $I_D$ = 1 mA, $V_{GS}$ = 0 | 1500 | | | V |
| $I_{DSS}$ | Zero gate voltage drain current ($V_{GS}$ = 0) | $V_{DS}$ = Max rating<br>$V_{DS}$ = Max rating, $T_C$=125 °C | | | 10<br>500 | µA<br>µA |
| $I_{GSS}$ | Gate-body leakage current ($V_{DS}$ = 0) | $V_{GS}$ = ± 30 V | | | ± 100 | nA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 3 | 4 | 5 | V |
| $R_{DS(on}$ | Static drain-source on resistance | $V_{GS}$ = 10 V, $I_D$ = 1.3 A | | 6 | 9 | Ω |

**Table 6. Dynamic**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $g_{fs}$ (1) | Forward transconductance | $V_{DS}$ = 30 V, $I_D$ = 1.3 A | | 2.6 | | S |
| $C_{iss}$<br>$C_{oss}$<br>$C_{rss}$ | Input capacitance<br>Output capacitance<br>Reverse transfer capacitance | $V_{DS}$ = 25 V, f = 1 MHz, $V_{GS}$ = 0 | | 939<br>102<br>13.2 | | pF<br>pF<br>pF |
| $C_{oss\ eq.}$ (2) | Equivalent output capacitance | $V_{DS}$=0 to 1200 V, $V_{GS}$ = 0 | | 100 | | pF |
| $R_g$ | Gate input resistance | f=1 MHz Gate DC Bias=0<br>Test signal level=20 mV<br>open drain | | 4 | | Ω |
| $Q_g$<br>$Q_{gs}$<br>$Q_{gd}$ | Total gate charge<br>Gate-source charge<br>Gate-drain charge | $V_{DD}$ = 1200 V, $I_D$ = 2.5 A,<br>$V_{GS}$ = 10 V | | 29.3<br>4.6<br>17 | | nC<br>nC<br>nC |

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%
2. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as $C_{oss}$ when $V_{DS}$ increases from 0 to 80% $V_{DSS}$

**Table 7. Switching times**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD}$ = 750 V, $I_D$ = 1.25 A, $R_G$ = 4.7 Ω, $V_{GS}$ = 10 V | | 24 | | ns |
| $t_r$ | Rise time | | | 47 | | ns |
| $t_{d(off)}$ | Turn-off-delay time | | | 45 | | ns |
| $t_f$ | Fall time | | | 61 | | ns |

**Table 8. Source drain diode**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$ | Source-drain current | | | | 2.5 | A |
| $I_{SDM}$ (1) | Source-drain current (pulsed) | | | | 10 | A |
| $V_{SD}$ (2) | Forward on voltage | $I_{SD}$ = 2.5 A, $V_{GS}$ = 0 | | | 1.6 | V |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 2.5 A, di/dt = 100 A/µs $V_{DD}$= 60 V | | 410 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | | 2.4 | | µC |
| $I_{RRM}$ | Reverse recovery current | | | 11.7 | | A |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 2.5 A, di/dt = 100 A/µs $V_{DD}$= 60 V, Tj = 150 °C | | 540 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | | 3.3 | | µC |
| $I_{RRM}$ | Reverse recovery current | | | 12.3 | | A |

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

**Figure 2. Safe operating area for TO-220**

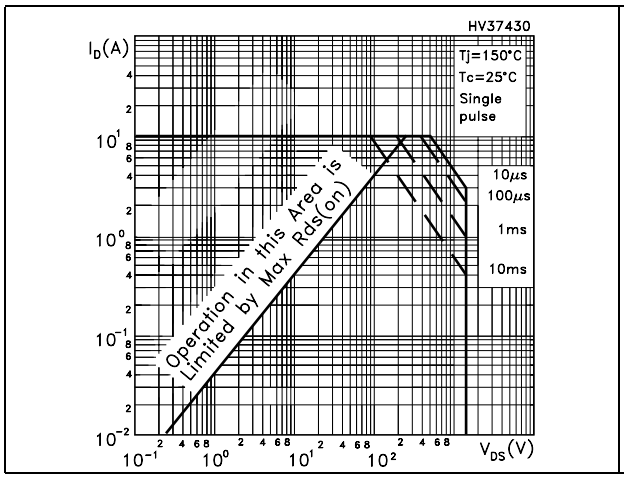



**Figure 3. Thermal impedance for TO-220**

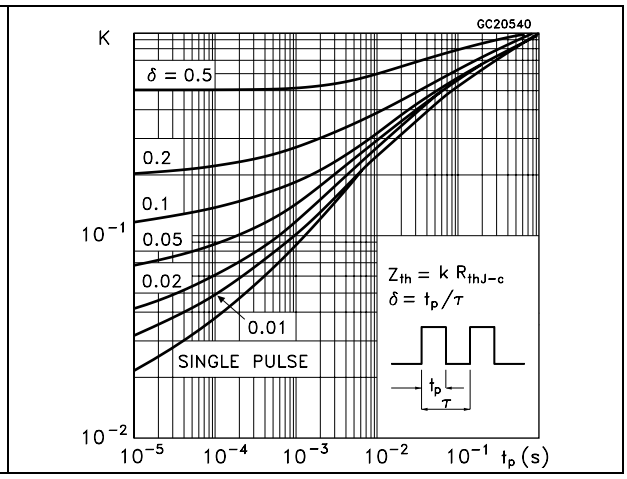



**Figure 4. Safe operating area for TO-220FH**

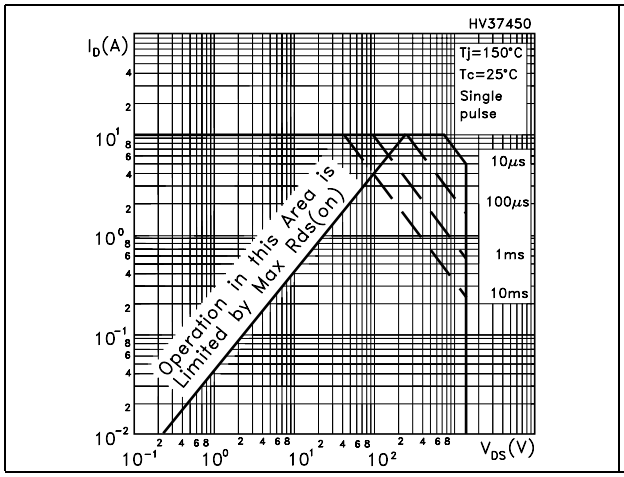



**Figure 5. Thermal impedance for TO-220FH**

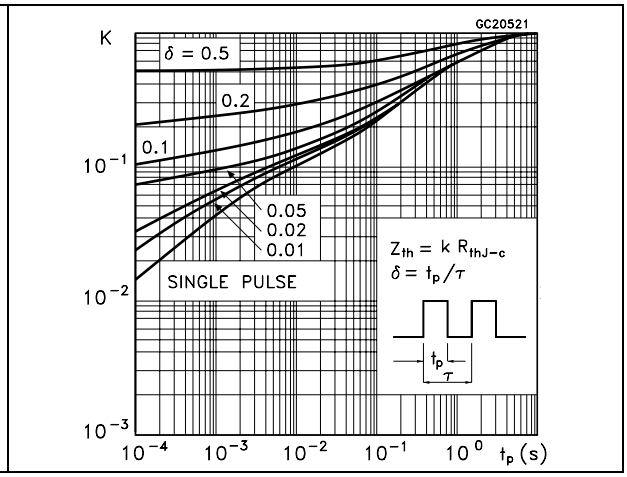



**Figure 6. Safe operating area for TO-247**

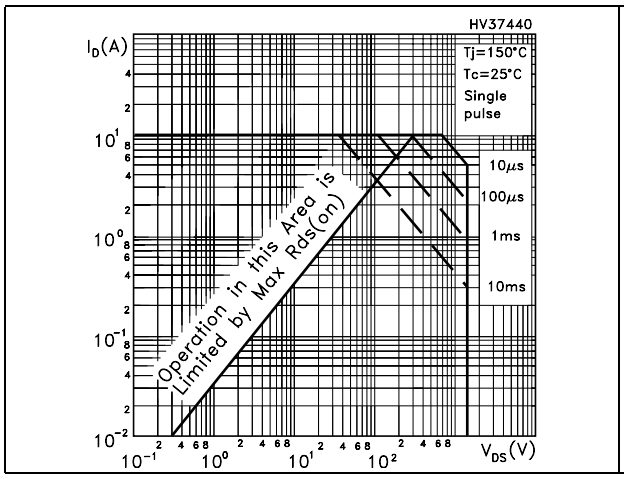



**Figure 7. Thermal impedance for TO-247**