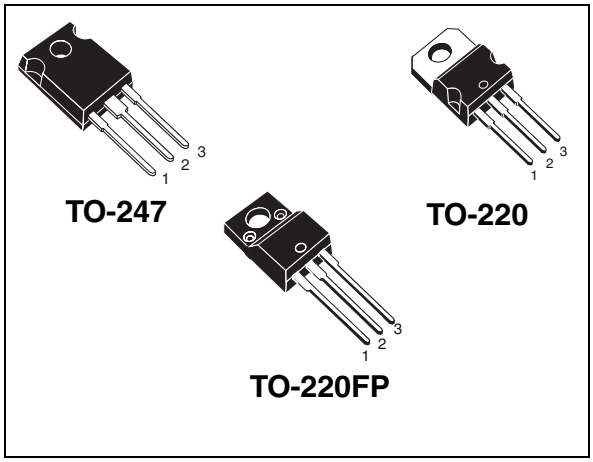
STF34NM60N
STP34NM60N, STW34NM60N

N-channel 600 V, 0.092 Ω, 29 A MDmesh™ II Power MOSFET
TO-220, TO-247, TO-220FP

Features

Type	V_{DSS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STF34NM60N	600 V	0.105 Ω	29 A	40 W
STP34NM60N	600 V	0.105 Ω	29 A	210 W
STW34NM60N	600 V	0.105 Ω	29 A	210 W

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance



Application

Switching applications

Description

These devices are made using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a new vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

Figure 1. Internal schematic diagram

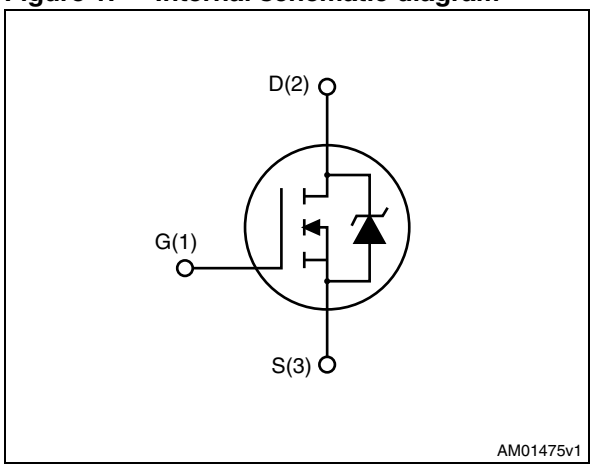


Table 1. Device summary

Order codes	Marking	Package	Packaging
STF34NM60N STP34NM60N STW34NM60N	34NM60N	TO-220FP TO-220 TO-247	Tube

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220, TO-247	TO-220FP	
V_{DS}	Drain-source voltage (V_{GS} = 0)	600		V
V_{GS}	Gate- source voltage	± 25		V
I_D	Drain current (continuous) at T_C = 25 °C	29	29 (1)	A
I_D	Drain current (continuous) at T_C = 100 °C	18	18	A
I_{DM} (2)	Drain current (pulsed)	116	116	A
P_{TOT}	Total dissipation at T_C = 25 °C	210	40	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max)	10.5		A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	345		mJ
dv/dt(3)	Peak diode recovery voltage slope	15		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; Tc = 25 °C)		1200	V
T_{stg}	Storage temperature	- 55 to 150		°C
T_J	Max. operating junction temperature	150		

1. Limited only by maximu temperature allowed.
2. Pulse width limited by safe operating area.
3. I_{SD} ≤ 29 A, di/dt ≤ 400 A/µs, V_{DS} peak ≤$V_{(BR)DSS}$, V_{DD} = 80% $V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	TO-220	TO-247	TO-220FP	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.60		3.13	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5	50	62.5	°C/W
T_l	Maximum lead temperature for soldering purpose	300			°C

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	600			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating V_{DS} = Max rating @125 °C			1 100	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 25 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 14.5 A		0.092	0.105	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0	-	2722 173 1.75	-	pF pF pF
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{GS} = 0, V_{DS} = 0 to 480 V	-	458	-	pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD} =300 V, I_D = 14.5 A R_G = 4.7 Ω, V_{GS} = 10 V	-	17 34 106 67	-	ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 480 V, I_D = 29 A, V_{GS} = 10 V,	-	83.6 14 45	-	nC nC nC
R_g	Gate input resistance	f=1MHz Gate DC Bias=0 Test signal level=20 mV Open drain	-	2.9	-	Ω

1. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)		-		29 116	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 29 A, V_{GS} = 0	-		1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 29 A, V_{DD} = 60 V di/dt=100 A/µs	-	408 8 39		ns nC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 29 A,V_{DD} = 60 V di/dt=100 A/µs, T_J = 150 °C	-	480 10 42		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220

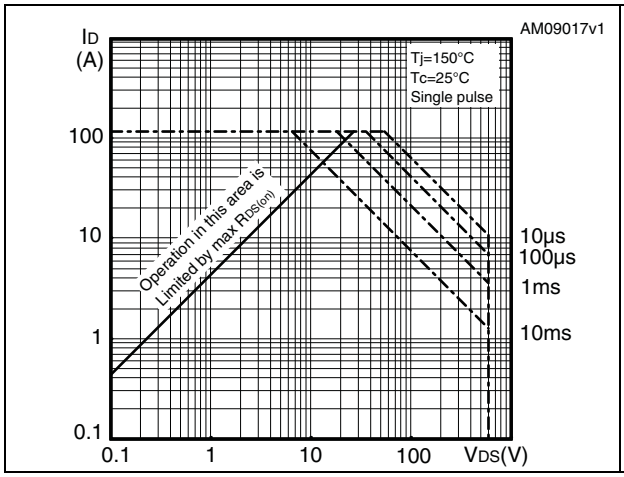


Figure 3. Thermal impedance for TO-220

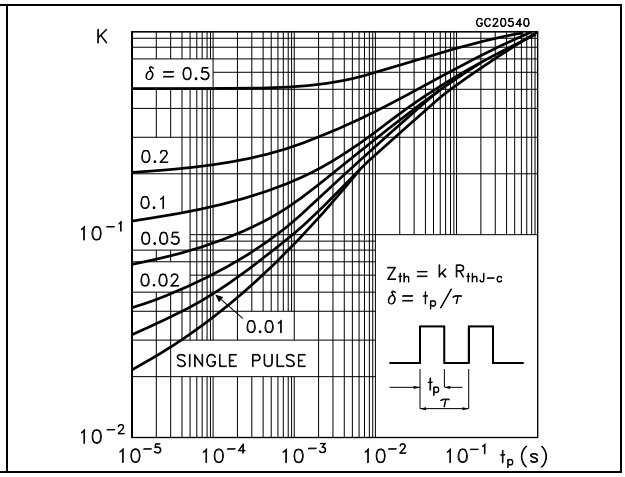


Figure 4. Safe operating area for TO-220FP

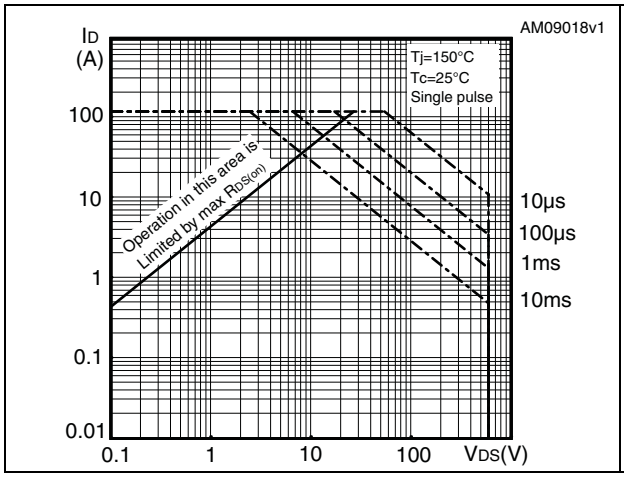


Figure 5. Thermal impedance for TO-220FP

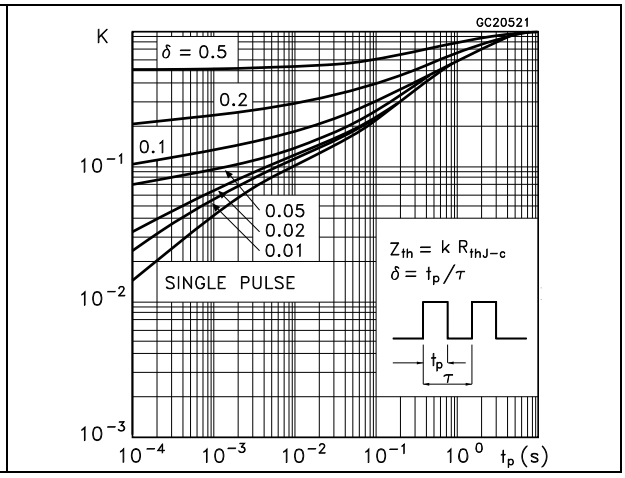


Figure 6. Safe operating area for TO-247

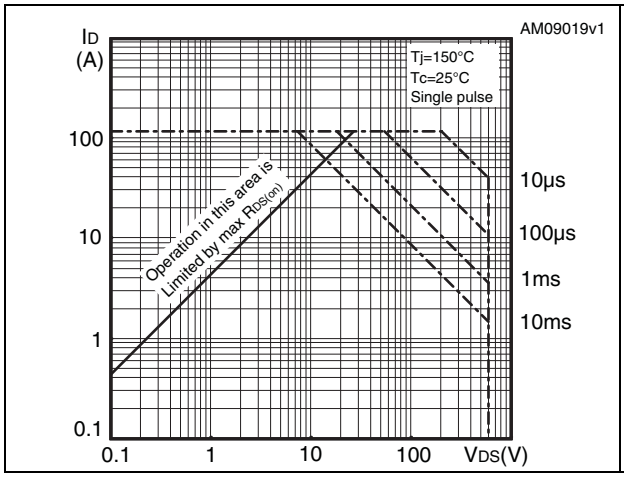


Figure 7. Thermal impedance for TO-247