STB30NM60N,STI30NM60N,STF30NM60N STP30NM60N, STW30NM60N

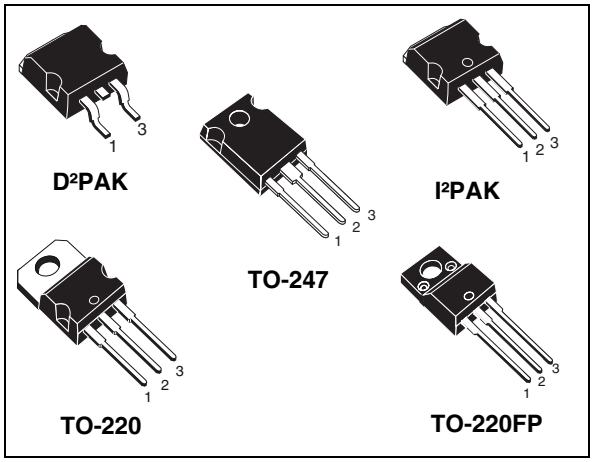
N-channel 600 V, 0.1 Ω, 25 A, MDmesh™ II Power MOSFET
TO-220, TO-220FP, TO-247, D²PAK, I²PAK

Features

Type	V_{DSS} @ T_{Jmax}	$R_{DS(on)}$ max	I_D	P_W
STB30NM60N	650 V	<0.13Ω	25A	190 W
STI30NM60N	650 V	<0.13Ω	25A	190 W
STF30NM60N	650 V	<0.13Ω	25A(1)	40 W
STP30NM60N	650 V	<0.13Ω	25A	190 W
STW30NM60N	650 V	<0.13Ω	25A	190 W

1. Limited only by maximum temperature allowed

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance



Application

- Switching applications

Description

This series of devices is designed using the second generation of MDmesh™ Technology. This revolutionary Power MOSFET associates a new vertical structure to the Company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

Figure 1. Internal schematic diagram

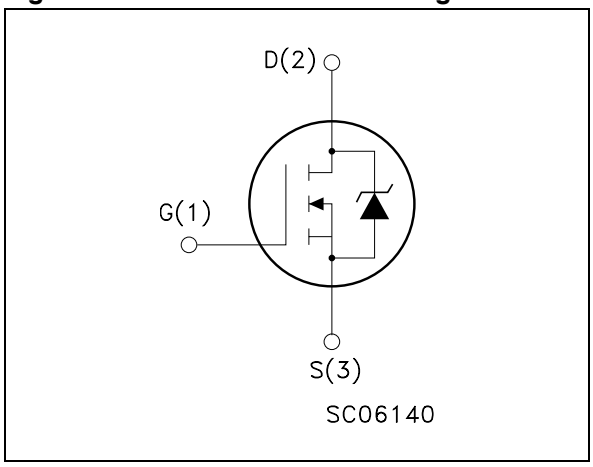


Table 1. Device summary

Order codes	Marking	Package	Packaging
STB30NM60N	30NM60N	D²PAK	Tape and reel
STI30NM60N	30NM60N	I²PAK	Tube
STF30NM60N	30NM60N	TO-220FP	Tube
STP30NM60N	30NM60N	TO-220	Tube
STW30NM60N	30NM60N	TO-247	Tube

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value					Unit
		TO-220	I²PAK	TO-247	D²PAK	TO-220FP	
V_{DS}	Drain-source voltage (V_{GS}=0)	600					V
V_{GS}	Gate-source voltage	± 30					V
I_D	Drain current (continuous) at T_C = 25 °C	25				25 (1)	A
I_D	Drain current (continuous) at T_C = 100 °C	15.8				15.8(1)	A
I_{DM} (2)	Drain current (pulsed)	100				100 (1)	A
P_{TOT}	Total dissipation at T_C = 25 °C	190				40	W
dv/dt (3)	Peak diode recovery voltage slope	15					V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s;T_C=25 °C)	--				2500	V
T_{stg}	Storage temperature	-55 to 150					°C
T_j	Max. operating juncion temperature	150					°C

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. $I_{SD} \leq$ 25A, di/dt $\leq$ 400A/µs, V_{DD} =80% $V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	TO-220	I²PAK	TO-247	D²PAK	TO-220FP	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.66				3.1	°C/W
$R_{thj-pcb}$	Thermal resistance junction-pcb max	--	--	--	30	--	°C/W
$R_{thj-amb}$	Thermal resistance junction-amb max	62.5		50	--	62.5	°C/W
T_l	Maximum lead temperature for soldering purposes	300					°C

Table 4. Avalanche characteristics

Symbol	Parameter	Max value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	12	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25°C, I_D = I_{AR}, V_{DD} = 50V)	900	mJ

2 Electrical characteristics

(Tcase =25°C unless otherwise specified)

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	600			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating V_{DS} = Max rating, T_C=125°C			1 100	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 12.5 A		0.1	0.13	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 15 V, I_D = 12.5 A		25		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0		2700 210 22		pF pF pF
$C_{oss\ eq.}$	Equivalent Output capacitance	V_{GS} = 0, V_{DS} = 0 to 480 V		66		pF
R_g	Gate input resistance	f=1MHz Gate DC Bias=0 Test signal level=20 mV open drain		3		Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} =480 V, I_D = 25 A, V_{GS} = 10 V		91 14 50		nC nC nC

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off-delay time Fall time	V_{DD} = 300 V, I_D = 12.5 A, R_G = 4.7 Ω, V_{GS} = 10 V		20 24 125 70		ns ns ns ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)				25 100	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 25 A, V_{GS} = 0			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 25 A, di/dt = 100 A/µs V_{DD}= 100 V		540 10 36		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 25 A, di/dt = 100 A/µs V_{DD}= 100 V Tj = 150°C		630 12 36		ns µC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220 / D²PAK / I²PAK

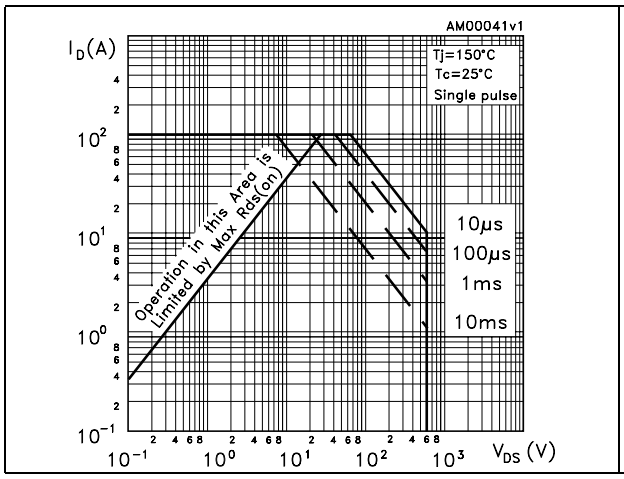


Figure 3. Thermal impedance for TO-220 / D²PAK / I²PAK

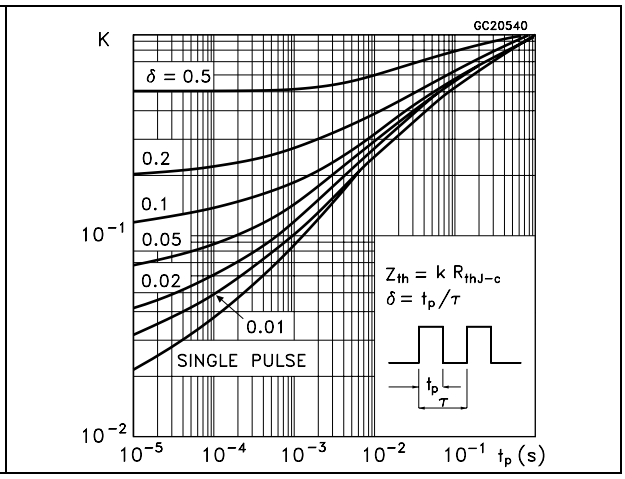


Figure 4. Safe operating area for TO-220FP

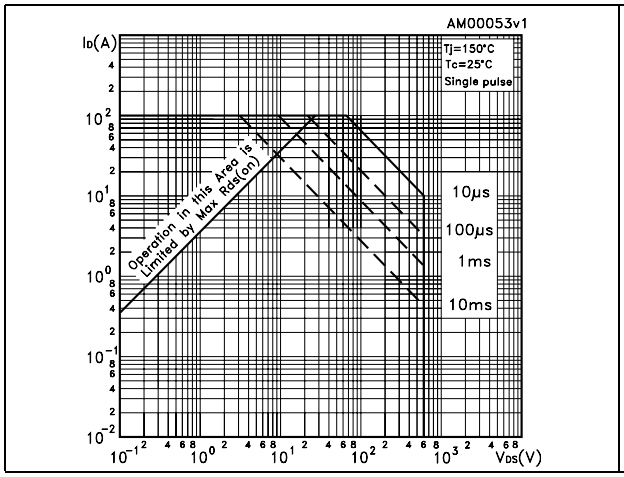


Figure 5. Thermal impedance for TO-220FP

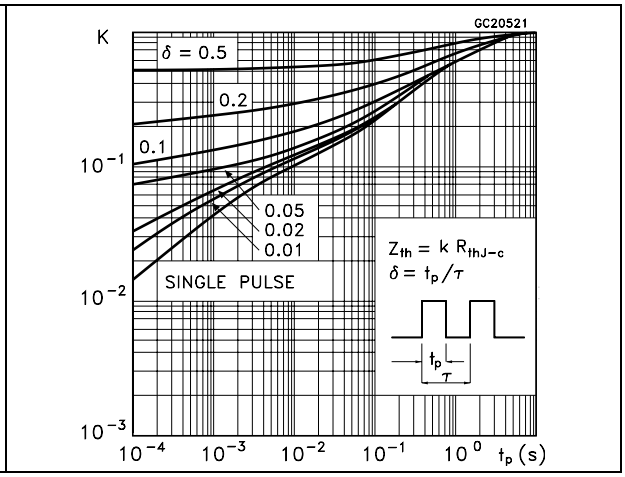


Figure 6. Safe operating area for TO-247

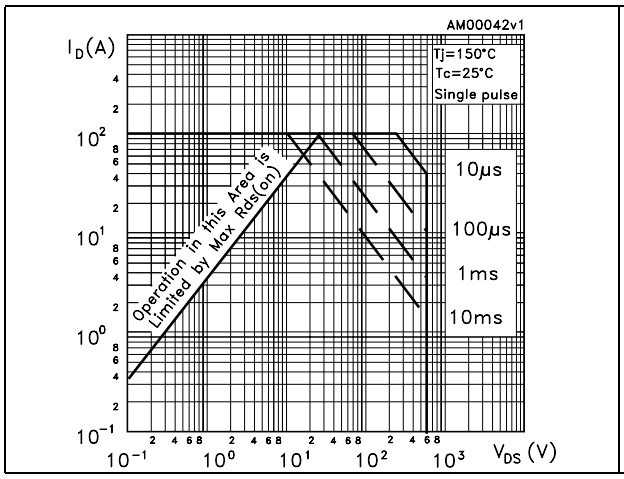


Figure 7. Thermal impedance for TO-247