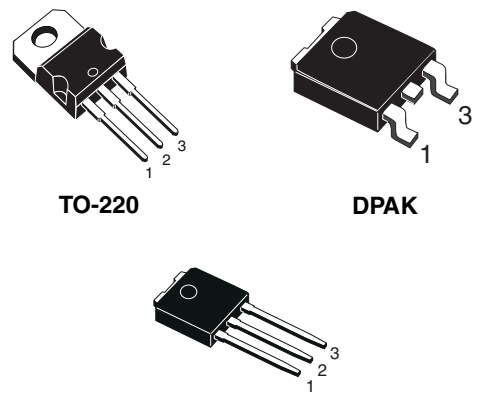
STP2NK90Z - STD2NK90Z
STD2NK90Z-1

N-channel 900V - 5Ω - 2.1A - TO-220 /DPAK/IPAK
Zener-Protected SuperMESH™ MOSFET

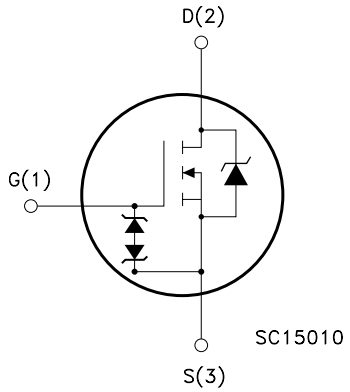
General features

Type	V_{DSS} (@Tjmax)	$R_{DS(on)}$	I_D	P_W
STD2NK90Z	900V	<6.5Ω	2.1A	70W
STD2NK90Z-1	900V	<6.5Ω	2.1A	70W
STP2NK90Z	900V	<6.5Ω	2.1A	70W

- Extremely high dv/dt capability
- Improved esd capability
- 100% avalanche rated
- Gate charge minimized
- Very low intrinsic capacitances
- Very good manufacturing repeatibility



Internal schematic diagram



Description

The SuperMESH™ series is obtained through an extreme optimization of ST's well established stripbased PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

Applications

- Switching application

Order codes

Part number	Marking	Package	Packaging
STD2NK90ZT4	D2NK90Z	DPAK	Tape & reel
STD2NK90Z-1	D2NK90Z	IPAK	Tube
STP2NK90Z	P2NK90Z	TO-220	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		STP2NK90Z	STD2NK90Z STD2NK90Z-1	
V_{DS}	Drain-source voltage (V_{GS} = 0)	900		V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 kΩ)	900		V
V_{GS}	Gate- source Voltage	± 30		V
I_D	Drain current (continuous) at T_C = 25°C	2.1		A
I_D	Drain current (continuous) at T_C = 100°C	1.3		A
I_{DM} (1)	Drain current (pulsed)	8.4		A
P_{TOT}	Total dissipation at T_C = 25°C	70		W
	Derating factor	0.56		W/°C
$V_{ESD(G-S)}$	Gate source ESD(HBM-C=100pF, R=1.5KΩ)	2000		V
dv/dt (2)	Peak diode recovery voltage slope	4.5		V/ns
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 150 -55 to 150		°C °C

1. Pulse width limited by safe operating area
2. $I_{SD} \leq$2.1A, di/dt $\leq$200A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
Rthj-case	Thermal resistance junction-case max	1.78	°C/W
Rthj-amb T_l	Thermal resistance junction-ambient max Maximum lead temperature for soldering purpose	62.5 300	°C/W °C

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	2.1	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	150	mJ

Table 4. Gate-source zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-source breakdown voltage	Igs=± 1mA (open drain)	30			V

1.1 Protection features of gate-to-source zener diodes

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test condictions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown Voltage	I_D = 1 mA, V_{GS} = 0	900			V
I_{DSS}	Zero gate voltage Drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating, T_C = 125°C			1 50	µA µA
I_{GSS}	Gate-body Leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			± 10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 50 µA	3	3.75	4.5	V
$R_{DS(on}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 1.05 A		5	6.5	Ω

Table 6. Dynamic

Symbol	Parameter	Test condictions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 15 V , I_D = 1.05 A		2.3		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0		485 50 10		pF pF pF
$C_{oss\ eq}$(2).	Equivalent output capacitance	V_{GS} = 0 V, V_{DS} = 0 to 720 V		24		pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 720 V, I_D = 2 A, V_{GS} = 10 V (see Figure 22)		19.5 3.4 10.8	27	nC nC nC

1. Pulsed: pulse duration=300µs, duty cycle 1.5%
2. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} inceases from 0 to 80% V_{DSS}

Table 7. Switching times

Symbol	Parameter	Test condictions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD} = 450 V, I_D = 1 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 19)		21 11 43 40		ns ns ns ns

Table 8. Source drain diode

Symbol	Parameter	Test condictions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current				2.1	A
I_{SDM}(1)	Source-drain current (pulsed)				8.4	A
V_{SD}(2)	Forward on voltage	I_{SD} = 2.1 A, V_{GS} = 0			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 2 A, di/dt = 100 A/µs V_{DD} = 50V (see Figure 20)		415 1.5 7.2		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 2 A, di/dt = 100 A/µs V_{DD} = 50V, T_j = 150°C (see Figure 20)		515 1.9 7.5		ns µC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300µs, duty cycle 1.5%