STH270N8F7-2, STH270N8F7-6, STP270N8F7

N-channel 80 V, 0.0017 Ω typ., 180 A, STripFET™ VII DeepGATE Power MOSFETs in H^{2}PAK-2, H^{2}PAK-6 and TO-220 packages

Datasheet — production data

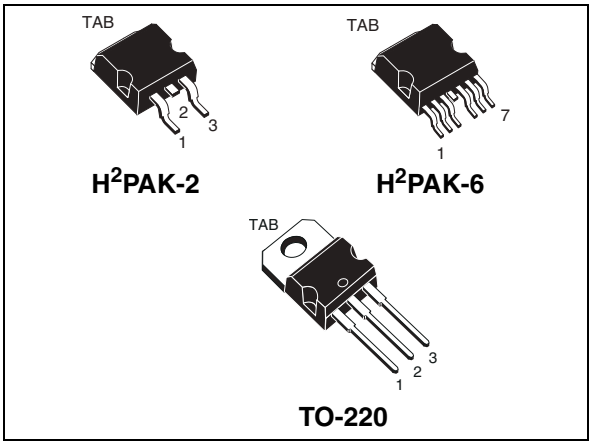
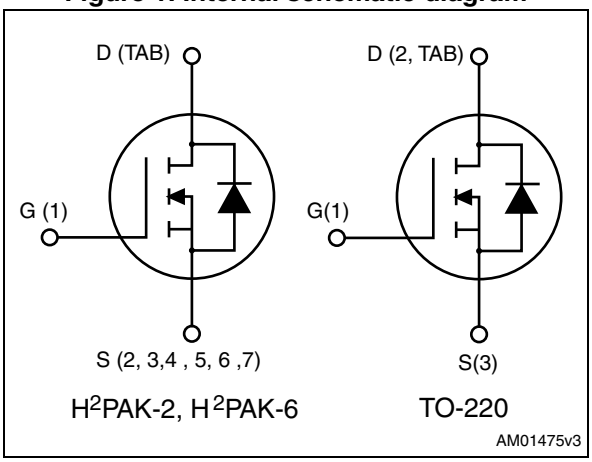


Figure 1. Internal schematic diagram



Features

Order codes	V_{DS}	$R_{DS(on)}$ max	I_D
STH270N8F7-2	80 V	0.0021 Ω	180 A
STH270N8F7-6			
STP270N8F7		0.0025 Ω	

- Ultra low on-resistance
- 100% avalanche tested

Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs developed using the 7th generation of STripFET™ DeepGATE™ technology, with a new gate structure. The resulting Power MOSFET exhibits the lowest $R_{DS(on)}$ in all packages.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STH270N8F7-2	270N8F7	H^{2}PAK-2	Tape and reel
STH270N8F7-6		H^{2}PAK-6	
STP270N8F7		TO-220	Tube

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	80	V
V_{GS}	Gate-source voltage	± 20	V
I_D (1)	Drain current (continuous)	180	A
I_D (1)	Drain current (continuous) at T_C = 100 °C	180	A
I_{DM} (2)	Drain current (pulsed)	720	A
P_{TOT} (3)	Total dissipation at T_C = 25 °C	315	W
E_{AS} (4)	Single pulse avalanche energy	1.16	J
T_J	Operating junction temperature	-55 to 175	°C
T_{stg}	Storage temperature		°C

1. Limited by package
2. Pulse width limited by safe operating area
3. This value is rated according to R_{thj-c}
4. Starting T_j = 25°C, I_d = 65 A, V_{dd} = 50 V

Table 3. Thermal resistance

Symbol	Parameter	Value		Unit
		H^2PAK-2, H^2PAK-6	TO-220	
$R_{thj-case}$	Thermal resistance junction-case	0.48		°C/W
$R_{thj-pcb}$ (1)	Thermal resistance junction-pcb	35		°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient max		62.5	°C/W

1. When mounted on FR-4 board of 1 $inch^2$, 2oz Cu

2 Electrical characteristics

(T_{CASE}=25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage (V_{GS}= 0)	I_D = 250 µA	80			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 80 V V_{DS} = 80 V; T_C=125 °C			10 100	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = +20 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	For H^2PAK-2, H^2PAK-6: V_{GS}= 10 V, I_D= 90 A		0.0017	0.0021	Ω
		For TO-220: V_{GS}= 10 V, I_D= 90 A		0.0021	0.0025	

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} =50 V, f=1 MHz, V_{GS}=0	-	13600	-	pF
C_{oss}	Output capacitance		-	2050	-	pF
C_{rss}	Reverse transfer capacitance		-	236	-	pF
Q_g	Total gate charge	V_{DD}=40 V, I_D = 180 A V_{GS} =10 V	-	193	-	nC
Q_{gs}	Gate-source charge		-	96	-	nC
Q_{gd}	Gate-drain charge		-	46	-	nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD}=40 V, I_D= 90 A, R_G=4.7 Ω, V_{GS}= 10 V	-	56	-	ns
t_r	Rise time		-	180	-	ns
$t_{d(off)}$	Turn-off delay time		-	98	-	ns
t_f	Fall time		-	42	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current		-		180	A
I_{SDM}(1)	Source-drain current (pulsed)		-		720	A
V_{SD}(2)	Forward on voltage	I_{SD} = 90 A, V_{GS}=0	-		1.2	V
t_{rr}	Reverse recovery time	I_{SD} = 180 A, di/dt = 100 A/µs, V_{DD}=64 V, T_j=150 °C	-	78		ns
Q_{rr}	Reverse recovery charge		-	182		nC
I_{RRM}	Reverse recovery current		-	4.7		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300µs, duty cycle 1.5%