

STB270N4F3

STI270N4F3 - STP270N4F3

N-channel 40 V - 2.1 mΩ - 160 A - TO-220 - D²PAK - I²PAK
STripFET™ Power MOSFET

Features

Type	V _{DSS}	R _{DS(on)} max	I _D	P _{TOT}
STB270N4F3	40 V	< 2.5 mΩ	160 A	330 W
STI270N4F3	40 V	< 2.9 mΩ	120 A	330 W
STP270N4F3	40 V	< 2.9 mΩ	120 A	330 W

- 100% avalanche tested
- Standard threshold drive

Applications

- High current, switching application
- Automotive

Description

This n-channel enhancement mode Power MOSFET is the latest refinement of STMicroelectronics unique “single feature size” strip-based process with less critical alignment steps and therefore a remarkable manufacturing reproducibility. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and low gate charge.

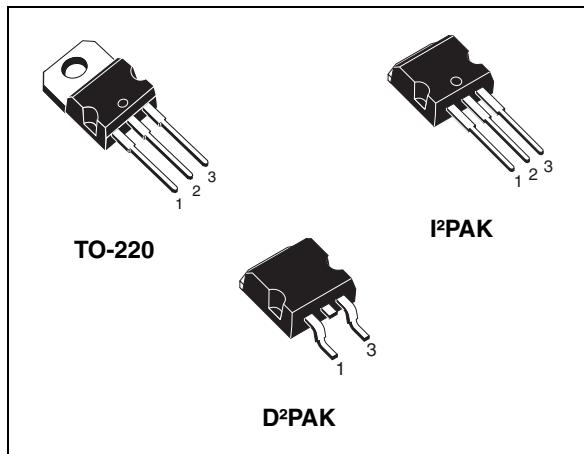


Figure 1. Internal schematic diagram

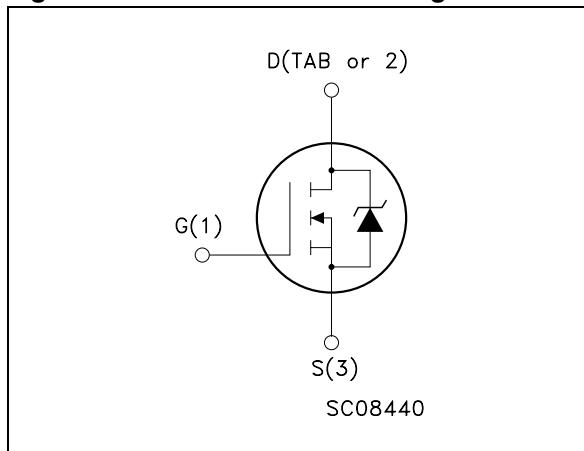


Table 1. Device summary

Order codes	Marking	Package	Packaging
STB270N4F3	270N4F3	D ² PAK	Tape and reel
STI270N4F3	270N4F3	I ² PAK	Tube
STP270N4F3	270N4F3	TO-220	Tube

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220/I ² PAK	D ² PAK	
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	40		V
V_{GS}	Gate-source voltage	± 20		V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	120	160	A
$I_D^{(1)}$	Drain current (continuous) at $T_C=100^\circ\text{C}$	120	160	A
$I_{DM}^{(2)}$	Drain current (pulsed)	480	640	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	330		W
	Derating factor	2.2		W/ $^\circ\text{C}$
$dv/dt^{(3)}$	Peak diode recovery voltage slope	3.5		V/n
$E_{AS}^{(4)}$	Single pulse avalanche energy	1		J
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 175		$^\circ\text{C}$

1. Current limited by package
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 120\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(\text{BR})DSS}$, $T_j \leq T_{JMAX}$
4. Starting $T_j=25^\circ\text{C}$, $I_D =80\text{A}$, $V_{DD}=32\text{V}$

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		TO-220/I ² PAK	D ² PAK	
$R_{thj-case}$	Thermal resistance junction-case max	0.45		$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max	--	35	$^\circ\text{C/W}$
R_{thj-a}	Thermal resistance junction-ambient max	62.5	--	$^\circ\text{C/W}$
T_I	Maximum lead temperature for soldering purpose (for 10 sec, 1.6 mm from case)	300	--	$^\circ\text{C}$

1. When mounted on 1inch² FR-4 board, 2 oz Cu.

2 Electrical characteristics

($T_{CASE}=25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}, V_{GS} = 0$		40			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$, $V_{DS} = \text{Max rating}$ $@125\text{ }^{\circ}\text{C}$				10 100	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$				± 200	nA
$V_{GS(\text{th})}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		2		4	V
$R_{DS(\text{on})}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}, I_D = 80\text{ A}$	TO-220		2.5	2.9	$\text{m}\Omega$
			I ² PAK		2.1	2.5	$\text{m}\Omega$

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15\text{ V}, I_D = 80\text{ A}$		200		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25\text{ V}, f = 1\text{ MHz}, V_{GS} = 0$		7400 1800 47		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge gate-drain charge	$V_{DD} = 20\text{ V}, I_D = 160\text{ A}$ $V_{GS} = 10\text{ V}$		110 27 25	150	nC nC nC

1. Pulsed: pulse duration=300 μs , duty cycle 1.5%

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	$V_{DD}=20\text{ V}$, $I_D=80\text{ A}$, $R_G=4.7\text{ }\Omega$, $V_{GS}=10\text{ V}$		22 180		ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	$V_{DD}=20\text{ V}$, $I_D=80\text{ A}$, $R_G=4.7\text{ }\Omega$, $V_{GS}=10\text{ V}$		110 45		ns ns

Table 7. Source drain diode

Symbol	Parameter		Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current	D²PAK				160	A
		TO-220 I²PAK				120	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)	D²PAK				640	A
		TO-220 I²PAK				480	A
$V_{SD}^{(2)}$	Forward on voltage		$I_{SD}=80\text{ A}$, $V_{GS}=0$			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current		$I_{SD}=160\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}$, $V_{DD}=32\text{ V}$, $T_j=150\text{ }^\circ\text{C}$		70 225 3.2		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 μs , duty cycle 1.5%