

STB26NM60ND, STF26NM60ND, STP26NM60ND, STW26NM60ND

N-channel 600 V, 0.145 Ω typ., 21 A, FDmesh™ II Power MOSFETs
in D²PAK, TO-220FP, TO-220 and TO-247 packages

Datasheet - production data

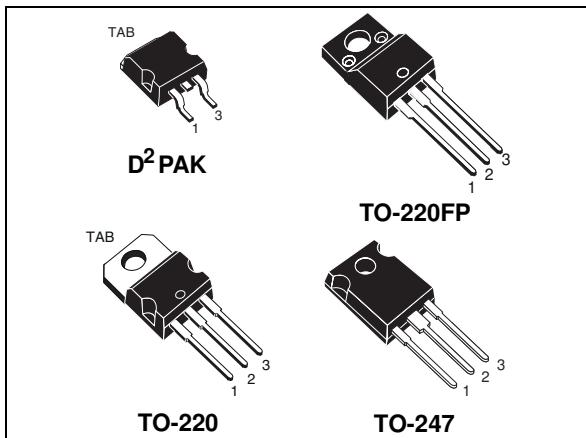
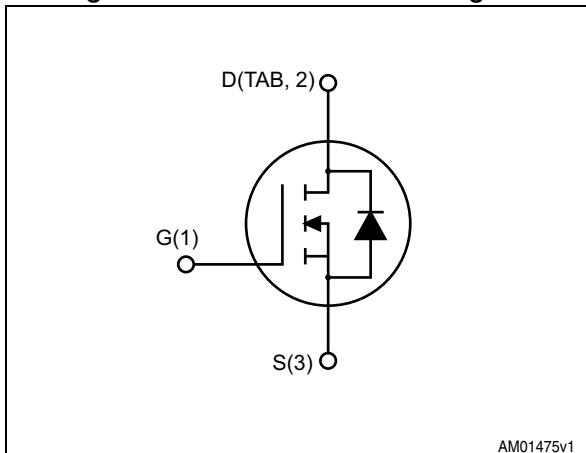


Figure 1. Internal schematic diagram



Features

Order codes	$V_{DS} @ T_{jmax}$	$R_{DS(on)} \text{ max}$	I_D
STB26NM60ND			
STF26NM60ND	650 V	0.175	
STP26NM60ND			
STW26NM60ND			21 A

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance
- Extremely high dv/dt and avalanche capabilities

Applications

- Switching applications

Description

These FDmesh™ II Power MOSFETs with intrinsic fast-recovery body diode are produced using the second generation of MDmesh™ technology. Utilizing a new strip-layout vertical structure, these revolutionary devices feature extremely low on-resistance and superior switching performance. They are ideal for bridge topologies and ZVS phase-shift converters.

Table 1. Device summary

Order codes	Marking	Packages	Packaging
STB26NM60ND	26NM60ND	D ² PAK	Tape and reel
STF26NM60ND		TO-220FP	Tube
STP26NM60ND		TO-220	
STW26NM60ND		TO-247	

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		D ² PAK, TO-220, TO-247	TO-220FP	
V _{DS}	Drain-source voltage	600		V
V _{GS}	Gate-source voltage	±25		V
I _D	Drain current (continuous) at T _C = 25 °C	21	21 ⁽¹⁾	A
I _D	Drain current (continuous) at T _C = 100 °C	13	13 ⁽¹⁾	A
I _{DM} ⁽²⁾	Drain current (pulsed)	84	84(1)	A
P _{TOT}	Total dissipation at T _C = 25 °C	190	35	W
dv/dt ⁽³⁾	Peak diode recovery voltage slope	40		V/ns
dv/dt ⁽⁴⁾	MOSFET dv/dt ruggedness	40		V/ns
V _{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s; T _C =25 °C)	2500		V
T _{stg}	Storage temperature	−55 to 150		°C
T _J	Max. operating junction temperature	150		°C

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. I_{SD} ≤ 21 A, di/dt ≤ 400 A/μs, V_{DD} = 80% V_{(BR)DSS}
4. V_{DS} ≤ 480 V

Table 3. Thermal data

Symbol	Parameter	Value				Unit
		D ² PAK	TO-220FP	TO-220	TO-247	
R _{thj-case}	Thermal resistance junction-case max	0.66	3.57	0.66		°C/W
R _{thj-amb}	Thermal resistance junction-ambient max		62.5	50		°C/W
R _{thj-pcb} ⁽¹⁾	Thermal resistance junction-pcb max	30				°C/W

1. When mounted on 1inch² FR-4 board, 2 oz Cu

Electrical ratings**STB26NM60ND, STF26NM60ND, STP26NM60ND, STW26NM60ND****Table 4. Avalanche characteristics**

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max)	4	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25$ °C, $I_D = I_{AS}$, $V_{DD} = 50$ V)	100	mJ

2 Electrical characteristics

($T_{CASE}=25\text{ }^{\circ}\text{C}$ unless otherwise specified).

Table 5. On/off states

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}, V_{GS} = 0$	600			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 600\text{ V}$ $V_{DS} = 600\text{ V} @ T_C = 125\text{ }^{\circ}\text{C}$			1 100	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 25\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on- resistance	$V_{GS} = 10\text{ V}, I_D = 10.5\text{ A}$		0.145	0.175	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}, f = 1\text{ MHz}, V_{GS} = 0$	-	1817	-	pF
C_{oss}	Output capacitance		-	90	-	pF
C_{rss}	Reverse transfer capacitance		-	4.4	-	pF
$C_{oss\ eq.}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0, V_{DS} = 0\text{ to }480\text{ V}$	-	270	-	pF
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}, I_D = 10.5\text{ A}$ $R_G = 4.7\text{ }\Omega$ $V_{GS} = 10\text{ V}$	-	22	-	ns
t_r	Rise time		-	14.5	-	ns
$t_{d(off)}$	Turn-off delay time		-	69	-	ns
t_f	Fall time		-	27.5	-	ns
Q_g	Total gate charge	$V_{DD} = 480\text{ V}, I_D = 21\text{ A}, V_{GS} = 10\text{ V}$	-	54.6	-	nC
Q_{gs}	Gate-source charge		-	9.1	-	nC
Q_{gd}	Gate-drain charge		-	32.5	-	nC
R_g	Intrinsic gate resistance	$f = 1\text{ MHz}, I_D = 0$	-	2.5	-	Ω

1. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		21	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		84	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 21 \text{ A}, V_{GS} = 0$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 21 \text{ A}, V_{DD} = 60 \text{ V}$ $dI/dt = 100 \text{ A}/\mu\text{s}$	-	170		ns
Q_{rr}	Reverse recovery charge		-	1.39		μC
I_{RRM}	Reverse recovery current		-	14		A
t_{rr}	Reverse recovery time	$I_{SD} = 21 \text{ A}, V_{DD} = 60 \text{ V}$ $dI/dt = 100 \text{ A}/\mu\text{s}$, $T_J = 150 \text{ }^\circ\text{C}$	-	230		ns
Q_{rr}	Reverse recovery charge		-	2.24		μC
I_{RRM}	Reverse recovery current		-	18		A

1. Pulse width limited by safe operating area
2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for D²PAK and TO-220

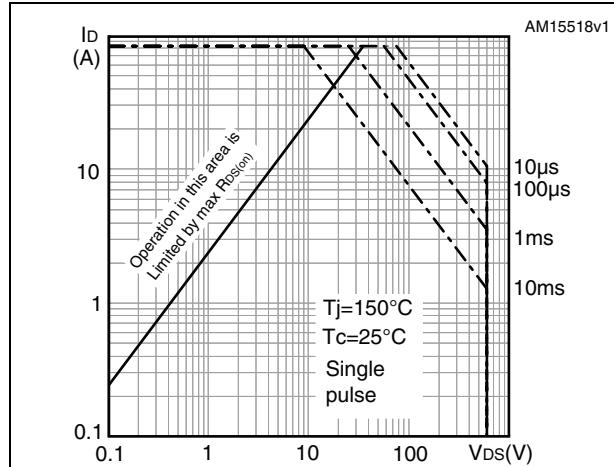


Figure 3. Thermal impedance for D²PAK and TO-220

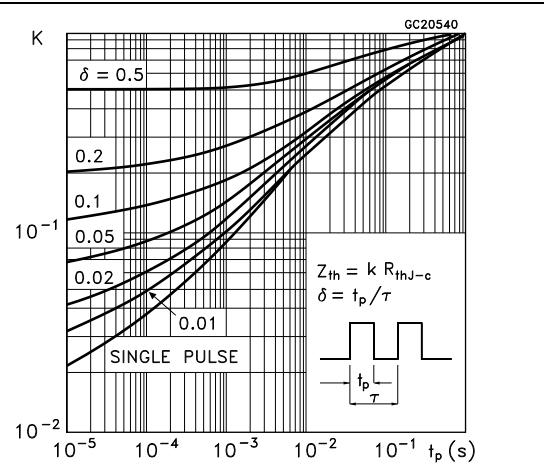


Figure 4. Safe operating area for TO-220FP

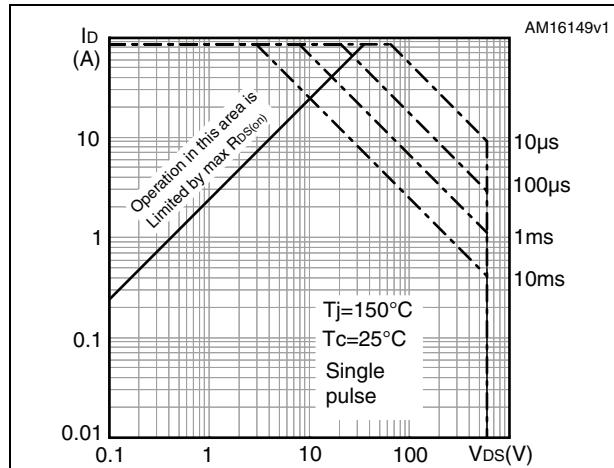


Figure 5. Thermal impedance for TO-220FP

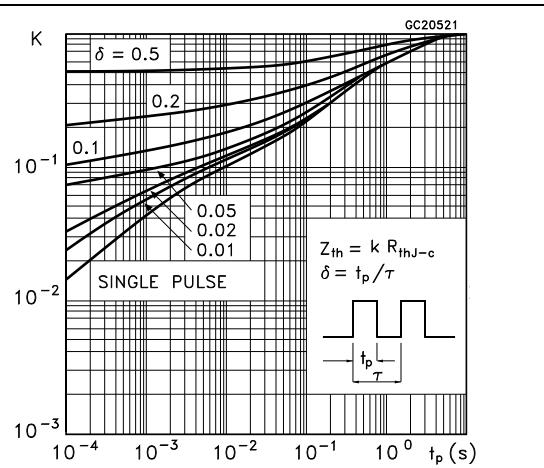


Figure 6. Safe operating area for TO-247

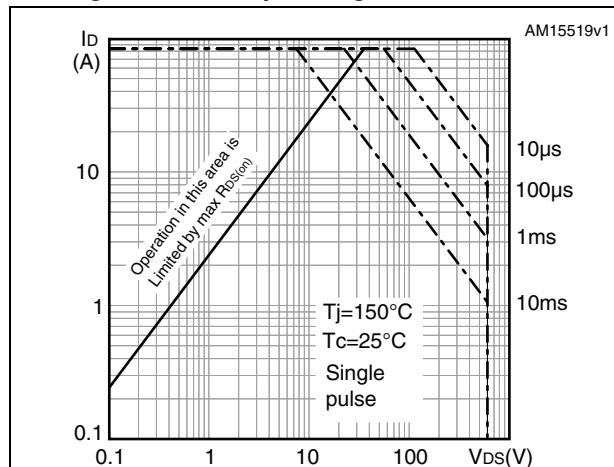


Figure 7. Thermal impedance for TO-247

