STx25NM60ND

N-channel 600 V, 0.13 Ω, 21 A FDmesh™ II Power MOSFET D²PAK, I²PAK, TO-220FP, TO-220, TO-247

Features

Type	V_{DSS} @ T_{JMAX}	$R_{DS(on)}$ max	I_D
STB25NM60ND	650 V	0.16 Ω	21 A
STI25NM60ND			21 A
STF25NM60ND			21 A(1)
STP25NM60ND			21 A
STW25NM60ND			21 A

1. Limited only by maximum temperature allowed

- The worldwide best $R_{DS(on)}$*area amongst the fast recovery diode devices
- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance
- Extremely high dv/dt and avalanche capabilities

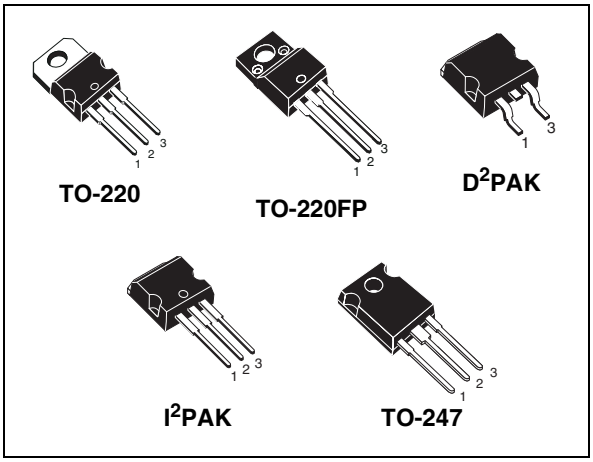
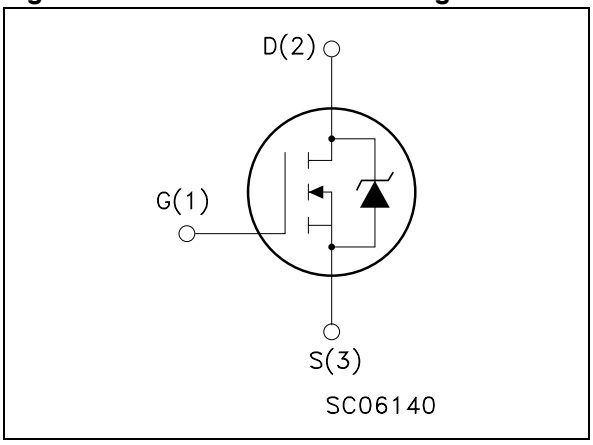


Figure 1. Internal schematic diagram



Application

- Switching applications

Description

The FDmesh™ II series belongs to the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a new vertical structure to the company's strip layout and associates all advantages of reduced on-resistance and fast switching with an intrinsic fast-recovery body diode.It is therefore strongly recommended for bridge topologies, in ZVS phase-shift converters.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STB25NM60ND	25NM60ND	D²PAK	Tape and reel
STI25NM60ND	25NM60ND	I²PAK	Tube
STF25NM60ND	25NM60ND	TO-220FP	Tube
STP25NM60ND	25NM60ND	TO-220	Tube
STW25NM60ND	25NM60ND	TO-247	Tube

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220, D^2PAK I^2PAK, TO-247	TO-220FP	
V_{DS}	Drain-source voltage (V_{GS} = 0)	600		V
V_{GS}	Gate-source voltage	±25		V
I_D	Drain current (continuous) at T_C = 25 °C	21	21(1)	A
I_D	Drain current (continuous) at T_C = 100 °C	13	13(1)	A
I_{DM} (2)	Drain current (pulsed)	84	84(1)	A
P_{TOT}	Total dissipation at T_C = 25 °C	160	40	W
dv/dt(3)	Peak diode recovery voltage slope	40		V/ns
Viso	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s;T_C=25 °C)		2500	V
T_{stg}	Storage temperature	–55 to 150		°C
T_J	Max. operating junction temperature	150		°C

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 21$ A, di/dt $\leq$ 600 A/µs, V_{DD} = 80% $V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	TO-220	I²PAK	TO-247	D²PAK	TO-220FP	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.78				3.1	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5		50		62.5	°C/W
$R_{thj-pcb}$	Thermal resistance junction-ambient max				30		°C/W
T_l	Maximum lead temperature for soldering purpose	300					°C

Table 4. Avalanche characteristics

Symbol	Parameter	Max value	Unit
I_{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max)	10	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AS}, V_{DD} = 50 V)	850	mJ

2 Electrical characteristics

(T_{CASE}=25 °C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	600			V
dv/dt(1)	Drain source voltage slope	V_{DD}= 480 V, I_D= 21 A, V_{GS}= 10 V		48		V/ns
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating V_{DS} = Max rating @125 °C			1 100	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 10.5 A		0.13	0.16	Ω

1. Characteristic value at turn off on inductive load

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 15 V, I_D = 10.5 A		17		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0		2400 150 15		pF pF pF
$C_{oss\ eq.}$(2)	Equivalent output capacitance	V_{GS} = 0, V_{DS} = 0 to 480 V		320		pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD} = 300 V, I_D = 10.5 A R_G = 4.7 Ω V_{GS} = 10 V		60 30 50 40		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 480 V, I_D = 21 A, V_{GS} = 10 V,		80 15 40		nC nC nC
R_g	Gate input resistance	f=1 MHz Gate DC Bias=0 Test signal level = 20 mV Open drain		1.6		Ω

1. Pulsed: pulse duration=300µs, duty cycle 1.5%
2. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)				21 84	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 21 A, V_{GS} = 0			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 21 A, V_{DD} = 60 V di/dt=100 A/µs		160 1 15		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 21 A,V_{DD} = 60 V di/dt=100 A/µs, T_J = 150 °C		230 2 19		ns µC A

1. Pulse width limited by safe operating area
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220, D²PAK, I²PAK

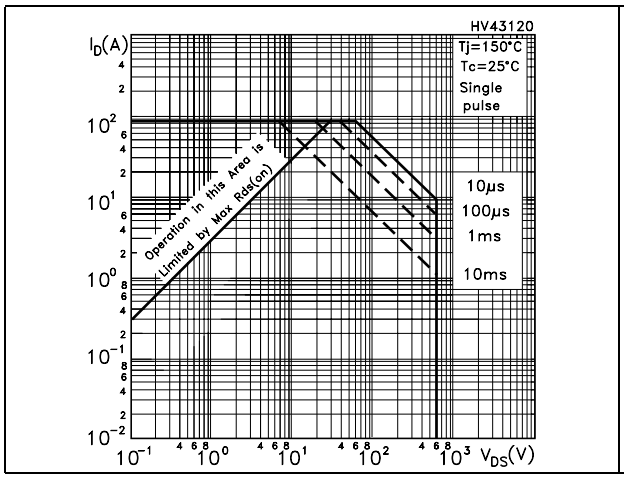


Figure 3. Thermal impedance for TO-220, D²PAK, I²PAK

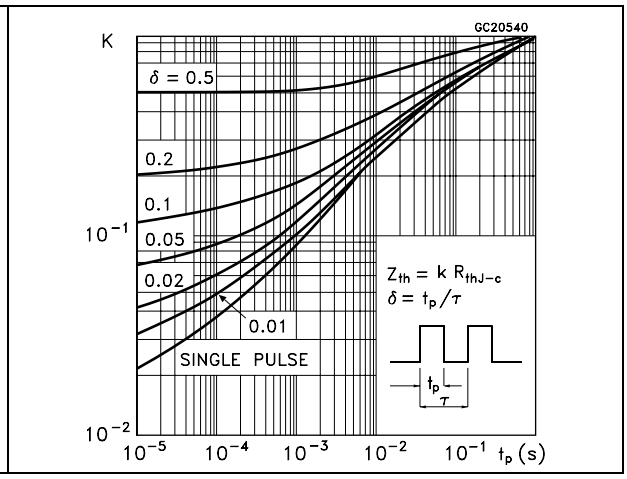


Figure 4. Safe operating area for TO-220FP

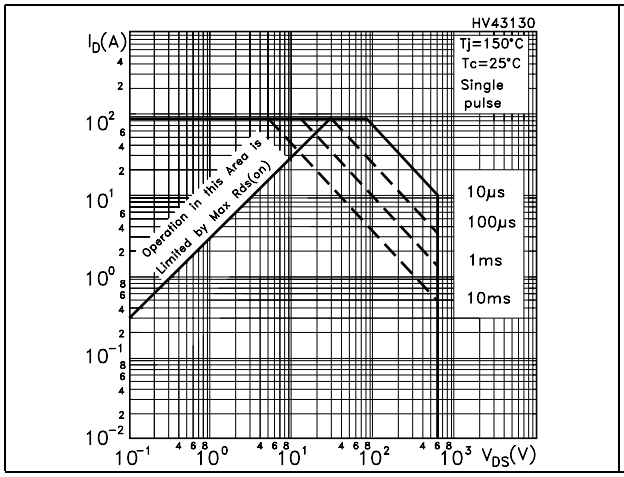


Figure 5. Thermal impedance for TO-220FP

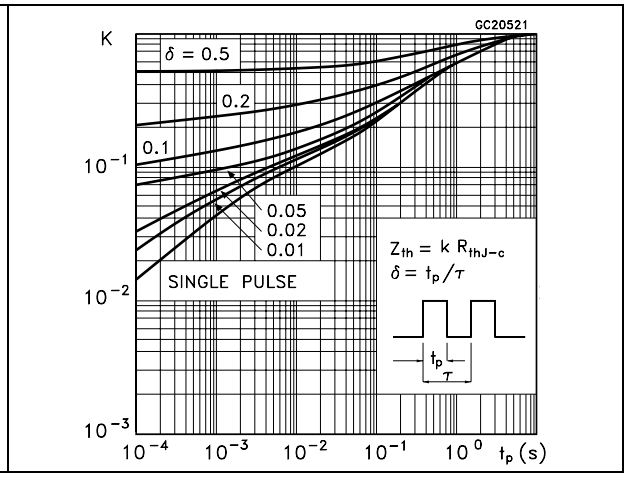


Figure 6. Safe operating area for TO-247

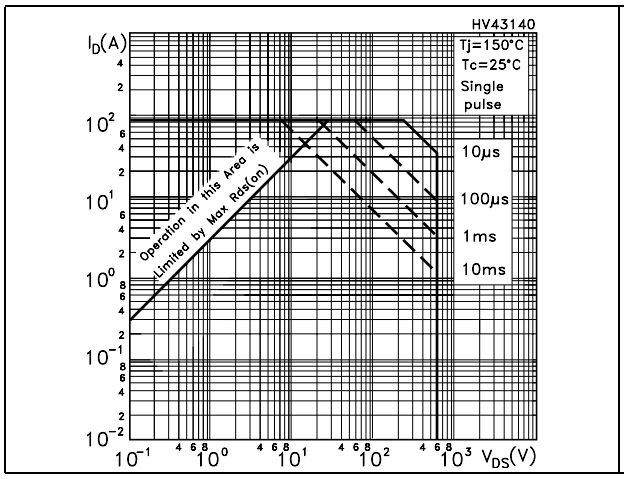


Figure 7. Thermal impedance for TO-247