STW24NM65N-STI24NM65N-STF24NM65N STB24NM65N - STP24NM65N

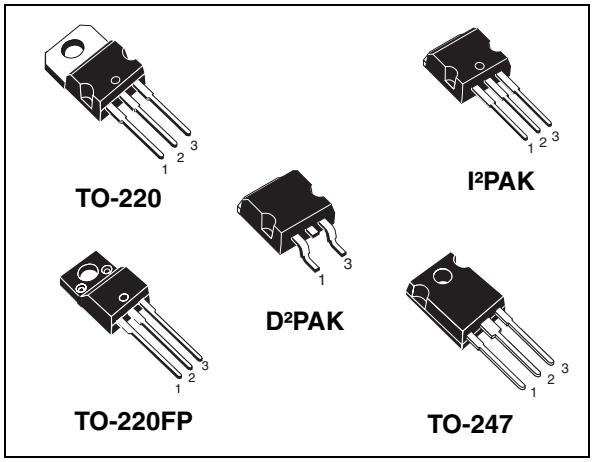
N-channel 650 V - 0.16 Ω - 19 A - TO-220 - TO-220FP - D^2PAK I^2PAK - TO-247 second generation MDmesh™ Power MOSFET

Features

Type	V_{DSS} (@$T_J$max)	$R_{DS(on)}$ max	I_D
STB24NM65N	710 V	< 0.19 Ω	19 A
STI24NM65N	710 V	< 0.19 Ω	19 A
STF24NM65N	710 V	< 0.19 Ω	19 A(1)
STP24NM65N	710 V	< 0.19 Ω	19 A
STW24NM65N	710 V	< 0.19 Ω	19 A

1. Limited only by maximum temperature allowed

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance



Application

- Switching applications

Description

This series of devices is designed using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a new vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

Figure 1. Internal schematic diagram

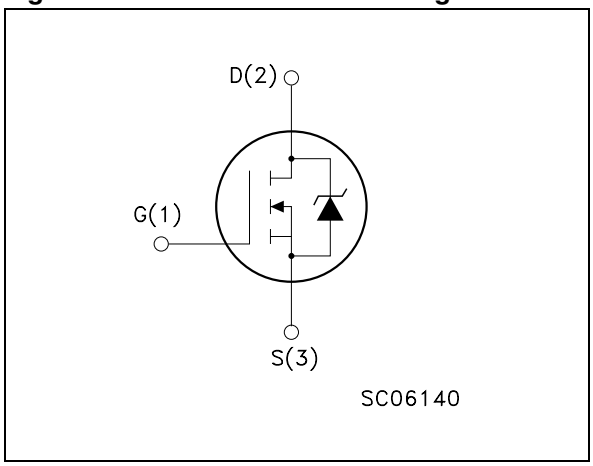


Table 1. Device summary

Order codes	Marking	Package	Packaging
STB24NM65N	24NM65N	D^2PAK	Tape and reel
STI24NM65N	24NM65N	I^2PAK	Tube
STF24NM65N	24NM65N	TO-220FP	Tube
STP24NM65N	24NM65N	TO-220	Tube
STW24NM65N	24NM65N	TO-247	Tube

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220/I²PAK TO-247/D²PAK	TO-220FP	
V_{DS}	Drain-source voltage (V_{GS}=0)	650		V
V_{GS}	Gate-source voltage	± 25		V
I_D	Drain current (continuous) at T_C = 25 °C	19	19(1)	A
I_D	Drain current (continuous) at T_C = 100 °C	12	12 (1)	A
I_{DM} (2)	Drain current (pulsed)	76	76(1)	A
P_{TOT}	Total dissipation at T_C = 25 °C	160	40	W
dv/dt (3)	Peak diode recovery voltage slope	15		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s;T_C=25 °C)	--	2500	V
T_{stg}	Storage temperature	-55 to 150		°C
T_J	Max. operating junction temperature	150		°C

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. I_{SD} ≤19 A, di/dt ≤400 A/µs, V_{DD} = 80% $V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	TO-220	I²PAK	TO-247	D²PAK	TO-220FP	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.78				3.1	°C/W
$R_{thj-amb}$	Thermal resistance junction-amb max	62.5		50	--	62.5	°C/W
$R_{thj-pcb}$	Thermal resistance junction-pcb max	--	--	--	30	--	°C/W
T_l	Maximum lead temperature for soldering purposes	300					°C

Table 4. Avalanche characteristics

Symbol	Parameter	Max value	Unit
I_{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max)	6	A
E_{AS}	Single pulse avalanche energy (starting T_J=25 °C, I_D=I_{AS}, V_{DD}= 50 V)	500	mJ

2 Electrical characteristics

(T_{CASE}=25 °C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	650			V
dv/dt (1)	Drain source voltage slope	V_{DD}= 520 V, I_D=19 A, V_{GS}=10 V		35		V/ns
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = max rating V_{DS} = max rating, @125 °C			1 100	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 9.5 A		0.16	0.19	Ω

1. Characteristic value at turn off on inductive load

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS}= 15 V, I_D = 9.5 A		14		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0		2500 120 10		pF pF pF
$C_{oss\ eq}$(2)	Equivalent output capacitance	V_{GS} = 0, V_{DS} = 0 to 520 V		310		pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 520 V, I_D = 19 A, V_{GS} = 10 V,		70 10 40		nC nC nC
R_G	Gate input resistance	f=1 MHz gate DC bias = 0 Test signal level = 20 mV open drain		2.5		Ω

1. Pulsed: pulse duration = 300µs, duty cycle 1.5%
2. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} =325 V, I_D = 9.5 A R_G = 4.7 Ω V_{GS} = 10 V		25		ns
t_r	Rise time			10		ns
$t_{d(off)}$	Turn-off delay time			80		ns
t_f	Fall time			20		ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
I_{SD}	Source-drain current				19	A
I_{SDM} (1)	Source-drain current (pulsed)				76	A
V_{SD} (2)	Forward on voltage	I_{SD} = 19 A, V_{GS} = 0			1.3	V
t_{rr}	Reverse recovery time	I_{SD} = 19 A, di/dt = 100 A/µs V_{DD} = 100 V		460		ns
Q_{rr}	Reverse recovery charge			7		µC
I_{RRM}	Reverse recovery current			30		A
t_{rr}	Reverse recovery time	I_{SD} = 19 A, di/dt = 100 A/µs V_{DD} = 100 V, T_J = 150 °C		620		ns
Q_{rr}	Reverse recovery charge			9		µC
I_{RRM}	Reverse recovery current			29		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220 - D²PAK - I²PAK

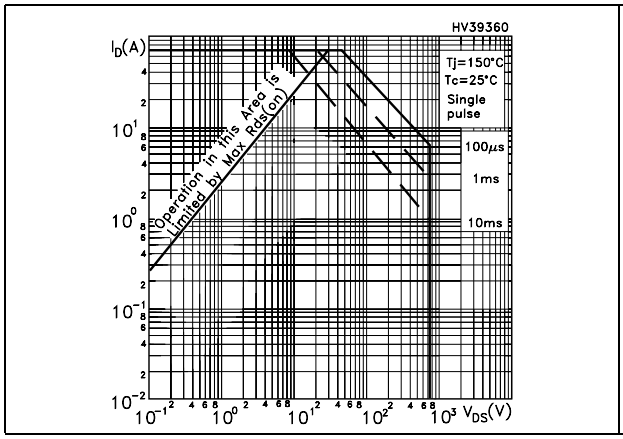


Figure 3. Thermal impedance for TO-220 - D²PAK - I²PAK

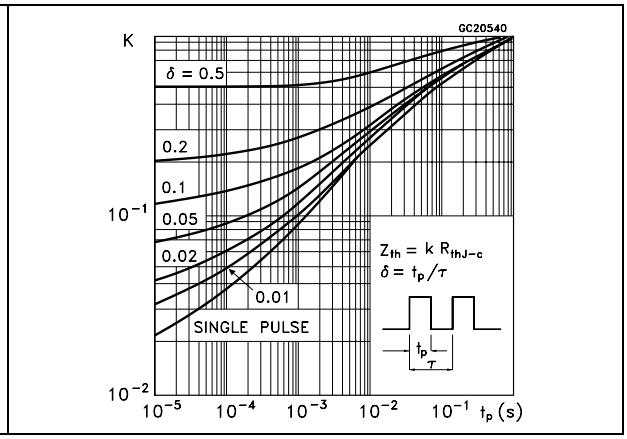


Figure 4. Safe operating area for TO-220FP

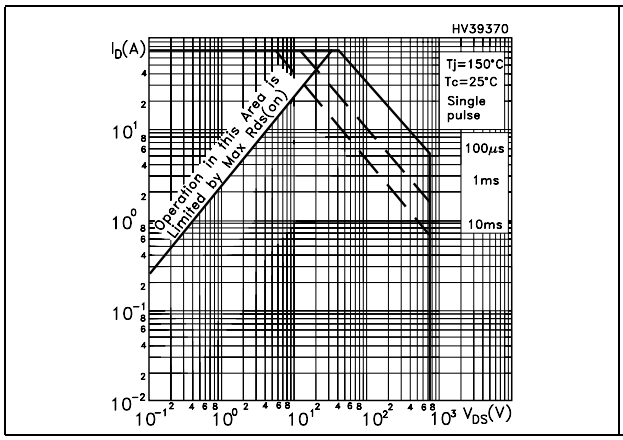


Figure 5. Thermal impedance for TO-220FP

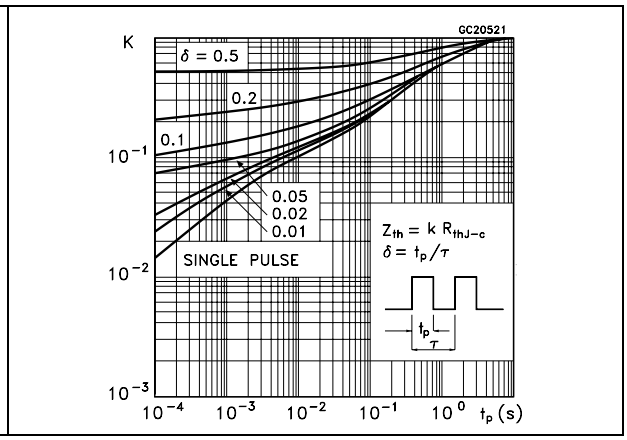


Figure 6. Safe operating area for TO-247

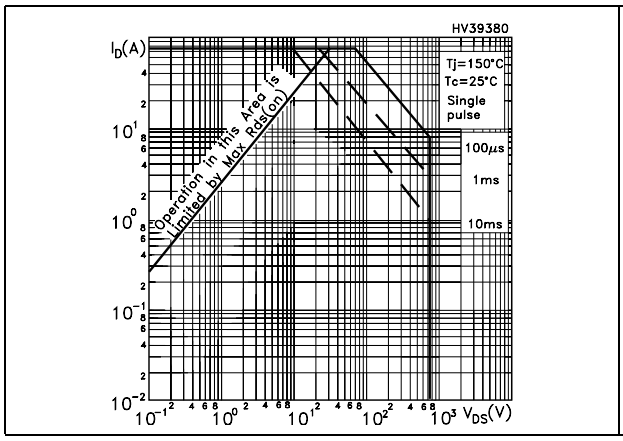


Figure 7. Thermal impedance for TO-247