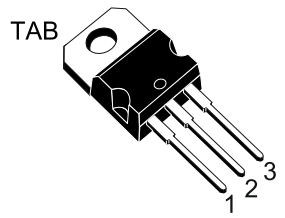
STP220N6F7

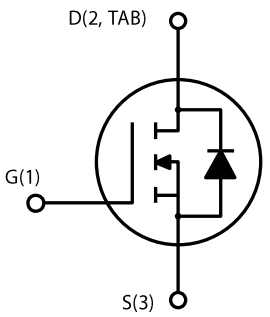
N-channel 60 V, 0.0021 Ω typ., 120 A, STripFET™ F7 Power MOSFET in a TO-220 package

Datasheet - production data



TO-220

Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)max}$	I_D	P_{TOT}
STP220N6F7	60 V	0.0024 Ω	120 A	237 W

- Among the lowest $R_{DS(on)}$ on the market
- Excellent figure of merit (FoM)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1: Device summary

Order code	Marking	Package	Packaging
STP220N6F7	220N6F7	TO-220	Tube

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	60	V
V_{GS}	Gate-source voltage	±20	V
I_D(1)	Drain current (continuous)	120	A
I_D(1)	Drain current (continuous) at T_C = 100 °C	120	A
I_{DM}(2)	Drain current (pulsed) T_C = 25 °C	480	A
P_{TOT}	Total dissipation at T_C = 25 °C	237	W
E_{AS}(3)	Single pulse avalanche energy	1	J
T_J	Operating junction temperature	-55 to 175	°C
T_{stg}	Storage temperature		°C

Notes:

(1)Current limited by package

(2)Pulse width is limited by safe operating area

(3)Starting T_j = 25°C, I_d = 20 A, V_{dd} = 50 V

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	0.63	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max	62.5	°C/W

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0, I_D = 1 mA	60			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0, V_{DS} = 60 V			1	µA
		V_{GS} = 0, V_{DS} = 60 V, T_C = 125 °C			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0, V_{GS} = + 20 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static drain-source on- resistance	V_{GS} = 10 V, I_D = 60 A		0.0021	0.0024	Ω

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	-	6400	-	pF
C_{oss}	Output capacitance		-	3880	-	pF
C_{rss}	Reverse transfer capacitance		-	175	-	pF
Q_g	Total gate charge	V_{DD} = 30 V, I_D = 120 A, V_{GS} = 10 V	-	100	-	nC
Q_{gs}	Gate-source charge		-	36	-	nC
Q_{gd}	Gate-drain charge		-	24	-	nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 30 V, I_D = 60 A, R_G = 4.7 Ω, V_{GS} = 10 V	-	33	-	ns
t_r	Rise time		-	103	-	ns
$t_{d(off)}$	Turn-off delay time		-	54	-	ns
t_f	Fall time		-	29	-	ns

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD}[1]	Forward on voltage	V_{GS} = 0, I_{SD} = 120 A	-	-	1.1	V
t_{rr}	Reverse recovery time	I_{SD} = 120 A, di/dt = 100 A/µs V_{DD} = 48 V, T_J = 150 °C	-	69		ns
Q_{rr}	Reverse recovery charge		-	104		nC
I_{RRM}	Reverse recovery current		-	3		A

Notes:

[1]Pulsed: pulse duration = 300 µs, duty cycle 1.5%