

STP/F21NM60ND-STW21NM60ND STB21NM60ND-STI21NM60ND

N-channel 600 V, 0.17 Ω , 17 A FDmesh™ II Power MOSFET
D²PAK, I²PAK, TO-220FP, TO-220, TO-247

Features

Type	V_{DSS} @ T_{Jmax}	$R_{DS(on)}$ max	I_D
STB21NM60ND	650 V	< 0.22 Ω	17 A
STI21NM60ND	650 V	< 0.22 Ω	17 A
STF21NM60ND	650 V	< 0.22 Ω	17 A ⁽¹⁾
STP21NM60ND	650 V	< 0.22 Ω	17 A
STW21NM60ND	650 V	< 0.22 Ω	17 A

1. Limited only by maximum temperature allowed
- The worldwide best $R_{DS(on)}$ *area amongst the fast recovery diode devices
 - 100% avalanche tested
 - Low input capacitance and gate charge
 - Low gate input resistance
 - Extremely high dv/dt and avalanche capabilities

Application

- Switching applications

Description

The FDmesh™ II series belongs to the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a new vertical structure to the company's strip layout and associates all advantages of reduced on-resistance and fast switching with an intrinsic fast-recovery body diode. It is therefore strongly recommended for bridge topologies, in ZVS phase-shift converters.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STB21NM60ND	21NM60ND	D ² PAK	Tape and reel
STI21NM60ND	21NM60ND	I ² PAK	Tube
STF21NM60ND	21NM60ND	TO-220FP	Tube
STP21NM60ND	21NM60ND	TO-220	Tube
STW21NM60ND	21NM60ND	TO-247	Tube

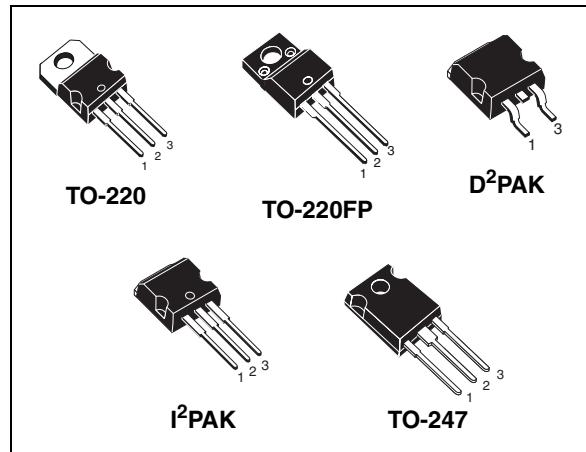


Figure 1. Internal schematic diagram

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220/D ² PAK I ² PAK / TO-247	TO-220FP	
V _{DS}	Drain-source voltage ($V_{GS} = 0$)	600		V
V _{GS}	Gate- source voltage	±25		V
I _D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	17	17 ⁽¹⁾	A
I _D	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	10	10 ⁽¹⁾	A
I _{DM} ⁽²⁾	Drain current (pulsed)	68	68 ⁽¹⁾	A
P _{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	140	30	W
dv/dt ⁽³⁾	Peak diode recovery voltage slope	40		V/ns
V _{iso}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t=1\text{ s}; T_C=25\text{ }^\circ\text{C}$)	--	2500	V
T _{stg}	Storage temperature	−55 to 150		°C
T _J	Max. operating junction temperature	150		

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 17\text{ A}$, $dI/dt \leq 600\text{ A}/\mu\text{s}$, $V_{DD} = 80\%$ $V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	TO-220	D ² PAK	I ² PAK	TO-247	TO-220FP	Unit
R _{thj-case}	Thermal resistance junction-case max			0.89		4.17	°C/W
R _{thj-amb}	Thermal resistance junction-ambient max	62.5	--	62.5	50	62.5	°C/W
T _I	Maximum lead temperature for soldering purpose			300			°C

Table 4. Avalanche characteristics

Symbol	Parameter	Max value	Unit
I _{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by T _J max)	8.5	A
E _{AS}	Single pulse avalanche energy (starting T _J = 25 °C, I _D = I _{AS} , V _{DD} = 50 V)	610	mJ

2 Electrical characteristics

($T_{CASE}=25^{\circ}\text{C}$ unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1 \text{ mA}, V_{GS} = 0$	600			V
$dv/dt^{(1)}$	Drain source voltage slope	$V_{DD} = 480 \text{ V}, I_D = 17 \text{ A}, V_{GS} = 10 \text{ V}$	48			V/ns
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating} @ 125^{\circ}\text{C}$			1 100	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20 \text{ V}$			100	nA
$V_{GS(\text{th})}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	3	4	5	V
$R_{DS(\text{on})}$	Static drain-source on resistance	$V_{GS} = 10 \text{ V}, I_D = 8.5 \text{ A}$		0.170	0.220	Ω

1. Characteristic value at turn off on inductive load

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15 \text{ V}, I_D = 8 \text{ A}$		12		s
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 50 \text{ V}, f = 1 \text{ MHz}, V_{GS} = 0$		1800 90 8		pF pF pF
$C_{oss \text{ eq.}}^{(2)}$	Equivalent output capacitance	$V_{GS} = 0, V_{DS} = 0 \text{ to } 480 \text{ V}$		300		pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	$V_{DD} = 300 \text{ V}, I_D = 8.5 \text{ A}$ $R_G = 4.7 \Omega, V_{GS} = 10 \text{ V}$		18 16 70 48		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 480 \text{ V}, I_D = 17 \text{ A}, V_{GS} = 10 \text{ V}$		60 10 30		nC nC nC
R_g	Gate input resistance	f=1 MHz Gate DC Bias=0 Test signal level=20 mV Open drain		3		Ω

1. Pulsed: pulse duration=300 μ s, duty cycle 1.5%

2. $C_{oss \text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current				17	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				68	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 17 \text{ A}, V_{GS} = 0$			1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 17 \text{ A}, V_{DD} = 60 \text{ V}$	150			ns
Q_{rr}	Reverse recovery charge	$dI/dt = 100 \text{ A}/\mu\text{s}$	0.90			μC
I_{RRM}	Reverse recovery current		13			A
t_{rr}	Reverse recovery time	$I_{SD} = 17 \text{ A}, V_{DD} = 60 \text{ V}$	210			ns
Q_{rr}	Reverse recovery charge	$dI/dt = 100 \text{ A}/\mu\text{s},$	1.6			μC
I_{RRM}	Reverse recovery current	$T_J = 150 \text{ }^\circ\text{C}$	15			A

1. Pulse width limited by safe operating area
2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220 / D²PAK / I²PAK

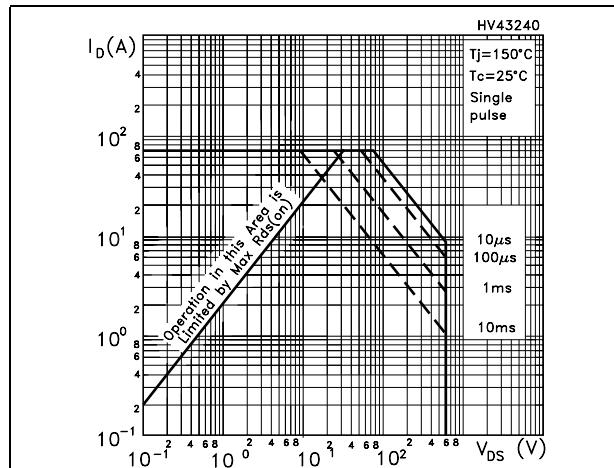


Figure 4. Safe operating area for TO-220FP

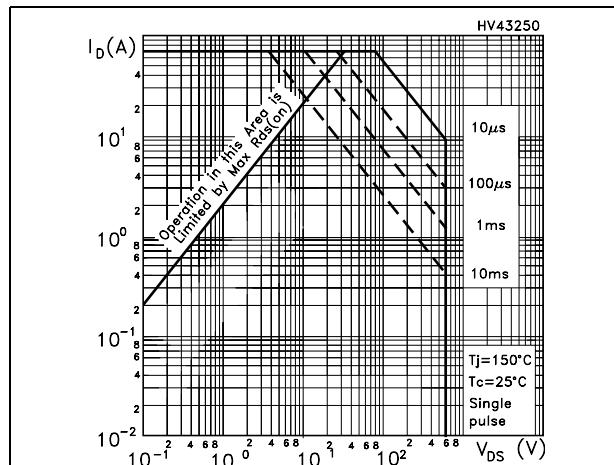


Figure 6. Safe operating area for TO-247

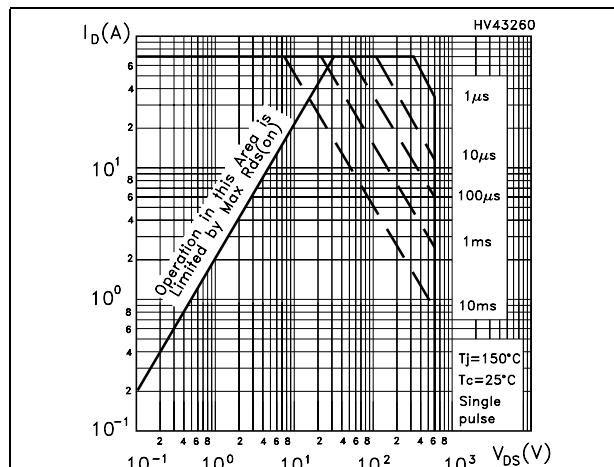


Figure 3. Thermal impedance for TO-220 / D²PAK / I²PAK

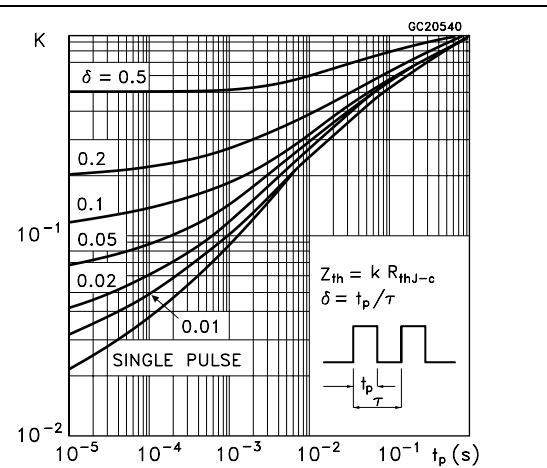


Figure 5. Thermal impedance for TO-220FP

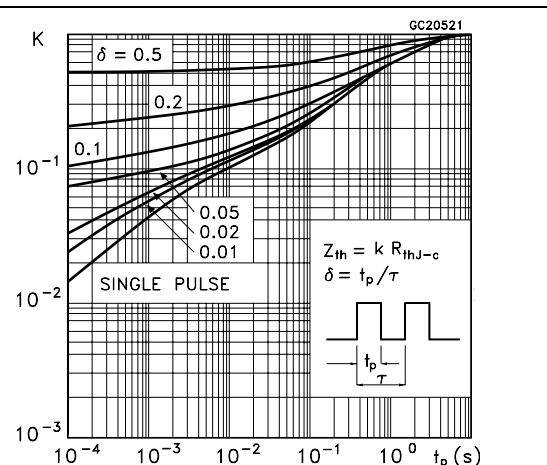


Figure 7. Thermal impedance for TO-247

