STP21NM50N-STF21NM50N-STW21NM50N
STB21NM50N - STB21NM50N-1

N-CHANNEL 500V - 0.15Ω - 18A TO-220/FP/D²/I²PAK/TO-247
SECOND GENERATION MDmesh™ MOSFET

Table 1: General Features

TYPE	V_{DSS} (@Tjmax)	$R_{DS(on)}$	I_D
STB21NM50N	550 V	< 0.19 Ω	18 A
STB21NM50N-1	550 V	< 0.19 Ω	18 A
STF21NM50N	550 V	< 0.19 Ω	18 A (*)
STP21NM50N	550 V	< 0.19 Ω	18 A
STW21NM50N	550 V	< 0.19 Ω	18 A

- 100% AVALANCHE TESTED
- LOW INPUT CAPACITANCE AND GATE CHARGE
- LOW GATE INPUT RESISTANCE

DESCRIPTION

The **STx21NM50N** is realized with the second generation of MDmesh Technology. This revolutionary MOSFET associates a new vertical structure to the Company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters

APPLICATIONS

The MDmesh™ II family is very suitable for increasing power density of high voltage converters allowing system miniaturization and higher efficiencies.

Figure 1: Package

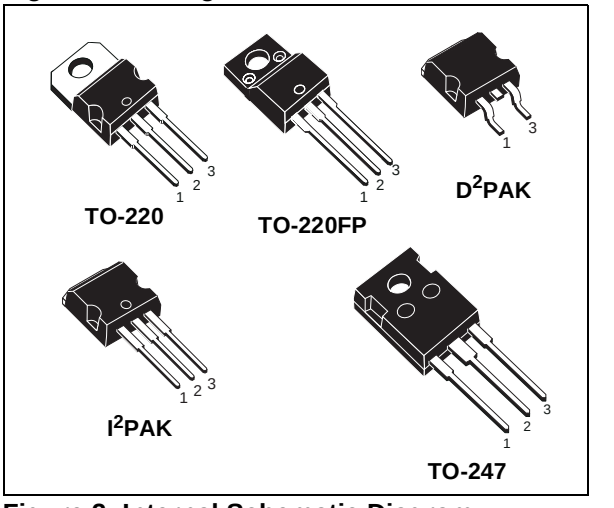

Figure 2: Internal Schematic Diagram

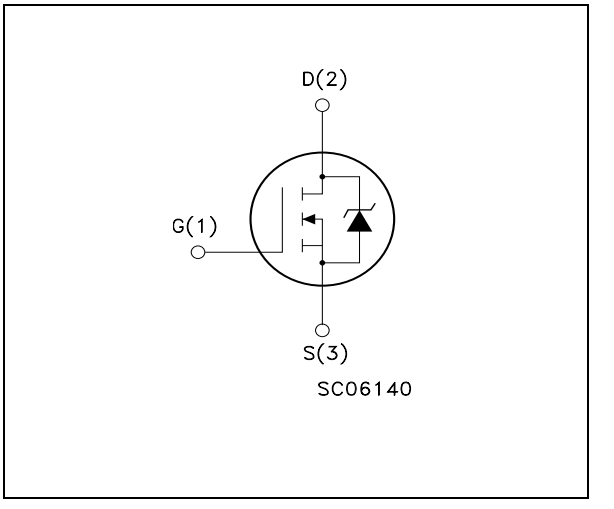

Table 2: Order Codes

SALES TYPE	MARKING	PACKAGE	PACKAGING
STB21NM50N	B21NM50N	D²PAK	TAPE & REEL
STB21NM50N-1	B21NM50N	I²PAK	TUBE
STF21NM50N	F21NM50N	TO-220FP	TUBE
STP21NM50N	P21NM50N	TO-220	TUBE
STW21NM50N	W21NM50N	TO-247	TUBE

Table 3: Absolute Maximum ratings

Symbol	Parameter	Value		Unit
		TO-220 / D^2PAK / I^2PAK / TO-247	TO-220FP	
V_{DS}	Drain-source Voltage (V_{GS} = 0)	500		V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	500		V
V_{GS}	Gate- source Voltage	±25		V
I_D	Drain Current (continuous) at T_C = 25°C	18	18 (*)	A
I_D	Drain Current (continuous) at T_C = 100°C	11	11 (*)	A
I_{DM} (•)	Drain Current (pulsed)	72	72 (*)	A
P_{TOT}	Total Dissipation at T_C = 25°C	140	30	W
	Derating Factor	1.12	0.23	W/°C
dv/dt(1)	Peak Diode Recovery voltage slope	15		V/ns
Viso	Insulation Winthstand Voltage (DC)	--	2500	V
T_{stg}	Storage Temperature	–55 to 150		°C
T_j	Max. Operating Junction Temperature	150		

(•) Pulse width limited by safe operating area
(*) Limited only by maximum temperature allowed
(1) $I_{SD} \leq 18$ A, di/dt ≤ 400 A/µs, V_{DD} =80% $V_{(BR)DSS}$

Table 4: Thermal Data

		TO-220 / D^2PAK / I^2PAK / TO-247	TO-220FP	
Rthj-case	Thermal Resistance Junction-case Max	0.89	4.21	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	62.5		°C/W
T_l	Maximum Lead Temperature For Soldering Purpose	300		°C

Table 5: Avalanche Characteristics

Symbol	Parameter	Max Value	Unit
I_{AS}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	9	A
E_{AS}	Single Pulse Avalanche Energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	480	mJ

ELECTRICAL CHARACTERISTICS (T_{CASE} =25°C UNLESS OTHERWISE SPECIFIED)

Table 6: On/Off

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 1mA, V_{GS} = 0	500			V
dv/dt(2)	Drain Source Voltage Slope	Vdd=400V, Id=25A, Vgs=10V		44		V/ns
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating T_C = 125 °C			1 10	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 20V			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10V, I_D = 9 A		0.150	0.190	Ω

(2) Characteristic value at turn off on inductive load

Table 7: Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	V_{DS} = 15 V, I_D = 9 A		12		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		1950 420 60		pF pF pF
$C_{oss\ eq.}$ (*)	Equivalent Output Capacitance	V_{GS} = 0V, V_{DS} = 0V to 400V		270		pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on Delay Time Rise Time Off-voltageRise Time Fall Time	V_{DD} =250 V, I_D = 9 A R_G = 4.7Ω V_{GS} = 10 V (see Figure 18)		22 18 90 30		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD} = 400V, I_D = 18 A, V_{GS} = 10V, (see Figure 21)		65 10 30		nC nC nC
R_g	Gate Input Resistance	f=1MHz Gate DC Bias=0 Test Signal Level=20mV Open Drain		1.6		Ω

(*) $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 8: Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}	Source-drain Current Source-drain Current (pulsed)				18 72	A A
V_{SD} (1)	Forward On Voltage	I_{SD} = 18 A, V_{GS} = 0			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 18 A, di/dt = 100 A/µs V_{DD} = 100 V, T_j = 25°C (see Figure 19)		360 5 27		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 18A, di/dt = 100 A/µs V_{DD} = 100 V, T_j = 150°C (see Figure 19)		640 6.5 27		ns µC A

Note: 1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.

Figure 3: Safe Operating Area For TO-220

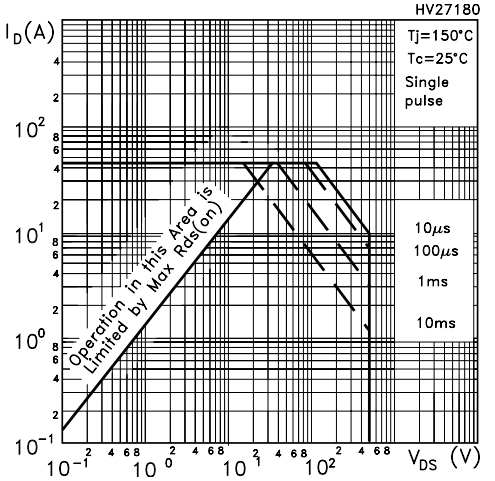

Figure 4: Safe Operating Area For TO-220FP

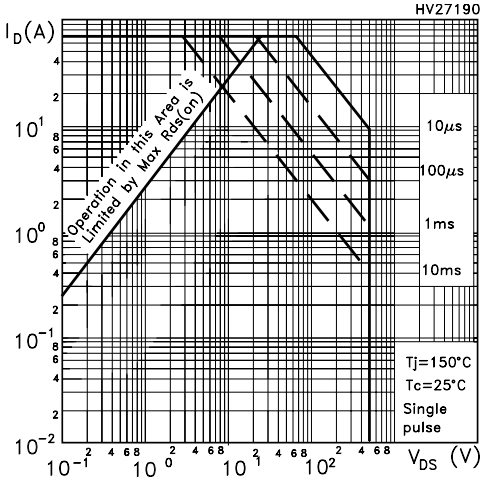

Figure 5: Output Characteristics

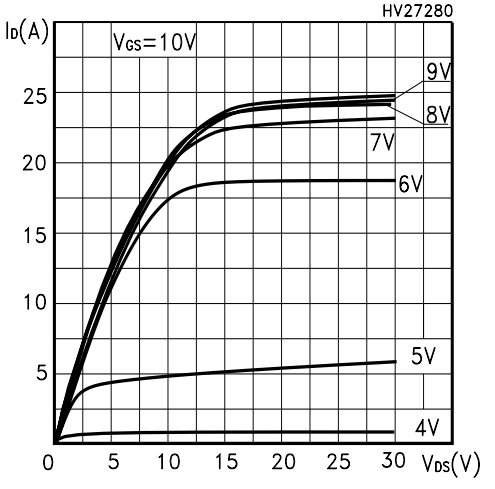

Figure 6: Thermal Impedance For TO-220

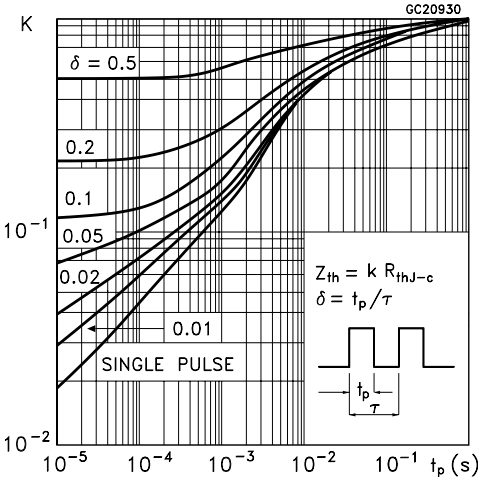

Figure 7: Thermal Impedance For TO-220FP

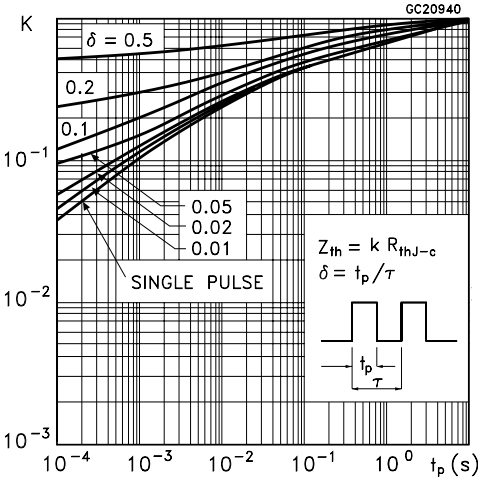

Figure 8: Transfer Characteristics