

STF19NM50N

STP19NM50N, STW19NM50N

N-channel 500 V, 0.2 Ω , 14 A MDmesh™ II Power MOSFET
in TO-220FP, TO-220 and TO-247

Features

Type	V_{DSS} @ T_{Jmax}	$R_{DS(on)}$ max	I_D
STF19NM50N	550 V	< 0.25 Ω	14 A
STP19NM50N			
STW19NM50N			

- 100% avalanche tested
- Low input capacitances and gate charge
- Low gate input resistance

Application

- Switching applications

Description

This second generation of MDmesh™ technology, applies the benefits of the multiple drain process to STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product offers improved on-resistance, low gate charge, high dv/dt capability and excellent avalanche characteristics.

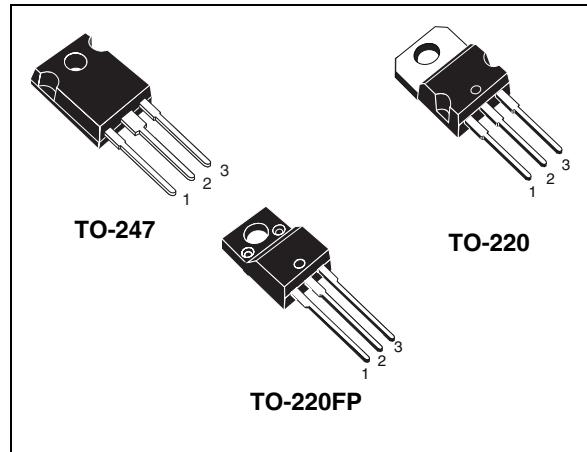


Figure 1. Internal schematic diagram

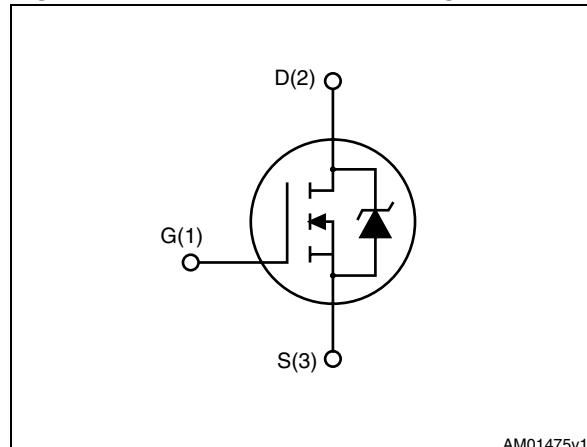


Table 1. Device summary

Order codes	Marking	Package	Packaging
STF19NM50N	19NM50N	TO-220FP	Tube
STP19NM50N		TO-220	
STW19NM50N		TO-247	

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value			Unit
		TO-220	TO-247	TO-220FP	
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	500			V
V_{GS}	Gate-source voltage	± 25			V
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$	14	14 ⁽¹⁾	A	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	9	9 ⁽¹⁾	A	A
I_{DM} ⁽²⁾	Drain current (pulsed)	56	56 ⁽¹⁾	A	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	110	30	W	
dv/dt ⁽³⁾	Peak diode recovery voltage slope	15			V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t = 1 \text{ s}; T_C = 25^\circ\text{C}$)			2500	V
T_{stg}	Storage temperature	- 55 to 150			$^\circ\text{C}$
T_j	Max. operating junction temperature	150			$^\circ\text{C}$

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 14 \text{ A}$, $dI/dt \leq 400 \text{ A}/\mu\text{s}$, $V_{Peak} < V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value			Unit
		TO-220	TO-247	TO-220FP	
$R_{thj-case}$	Thermal resistance junction-case max	1.14		4.17	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5	50	62.5	$^\circ\text{C}/\text{W}$
T_I	Maximum lead temperature for soldering purpose	300			$^\circ\text{C}$

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	7	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50 \text{ V}$)	208	mJ

2 Electrical characteristics

($T_C = 25^\circ\text{C}$ unless otherwise specified)

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$I_D = 1 \text{ mA}, V_{GS} = 0$	500			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating}, T_C = 125^\circ\text{C}$			1 10	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 25 \text{ V}$			10	μA
$V_{GS(\text{th})}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	2	3	4	V
$R_{DS(\text{on})}$	Static drain-source on resistance	$V_{GS} = 10 \text{ V}, I_D = 7 \text{ A}$		0.2	0.25	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance					pF
C_{oss}	Output capacitance					pF
C_{rss}	Reverse transfer capacitance	$V_{DS} = 50 \text{ V}, f = 1 \text{ MHz}, V_{GS} = 0$	-	1000 72 3	-	pF
$C_{o(\text{tr})}^{(1)}$	Equivalent capacitance time related		-	104	-	pF
$C_{o(\text{er})}^{(2)}$	Equivalent capacitance energy related	$V_{DS} = 0 \text{ to } 400 \text{ V}, V_{GS} = 0$	-	51	-	pF
R_G	Intrinsic gate resistance	$f = 1 \text{ MHz open drain}$	-	4.4	-	Ω
Q_g	Total gate charge	$V_{DD} = 400 \text{ V}, I_D = 14 \text{ A}, V_{GS} = 10 \text{ V}$		34		nC
Q_{gs}	Gate-source charge		-	5	-	nC
Q_{gd}	Gate-drain charge			18		nC

1. Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
2. Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 250 \text{ V}, I_D = 7 \text{ A}, R_G = 4.7 \Omega, V_{GS} = 10 \text{ V}$	-	12	-	ns
t_r	Rise time			16	-	ns
$t_{d(off)}$	Turn-off-delay time			61	-	ns
t_f	Fall time			17	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM}^{(1)}$	Source-drain current		-		14	A
	Source-drain current (pulsed)				56	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 14 \text{ A}, V_{GS} = 0$	-		1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 14 \text{ A}, dI/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$	-	296 3.5 23		ns nC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 14 \text{ A}, dI/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}, T_j = 150^\circ\text{C}$	-	346 4 24		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220

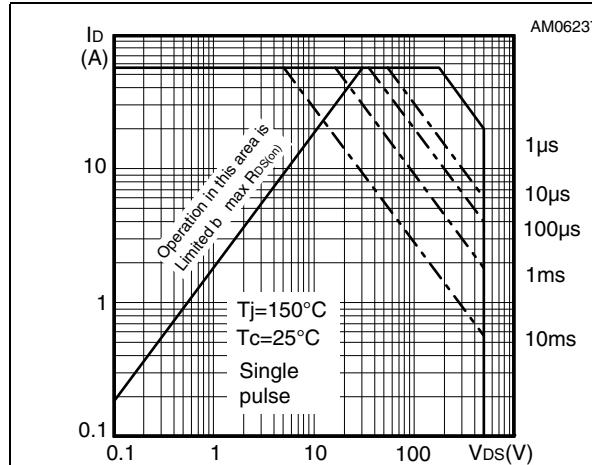


Figure 3. Thermal impedance for TO-220

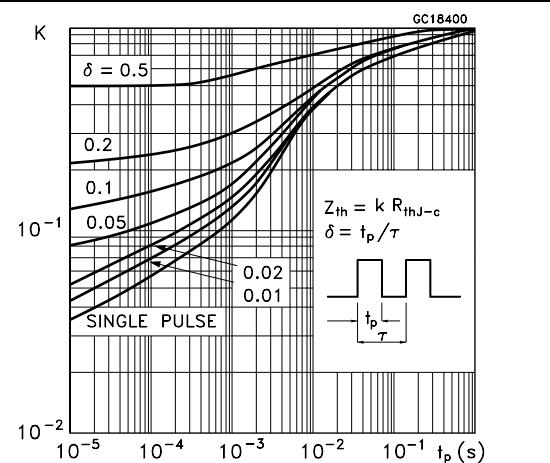


Figure 4. Safe operating area for TO-220FP

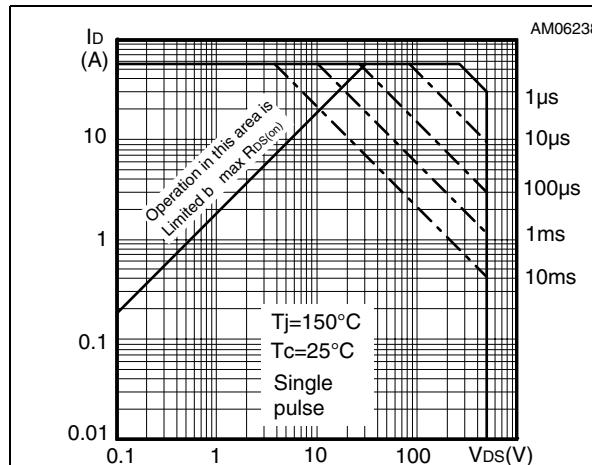


Figure 5. Thermal impedance for TO-220FP

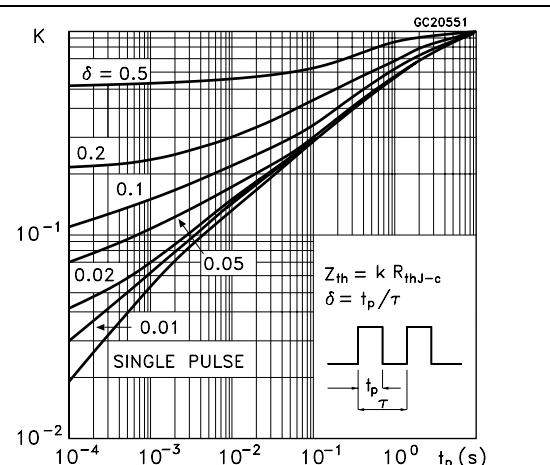


Figure 6. Safe operating area for TO-247

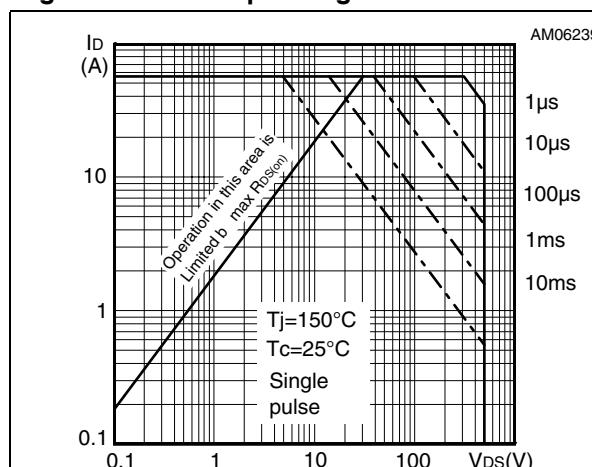


Figure 7. Thermal impedance for TO-247

