STB18NM80, STF18NM80, STP18NM80, STW18NM80

N-channel 800 V, 0.25 Ω, 17 A, MDmesh™ Power MOSFET in D²PAK, TO-220FP, TO-220 and TO-247 packages

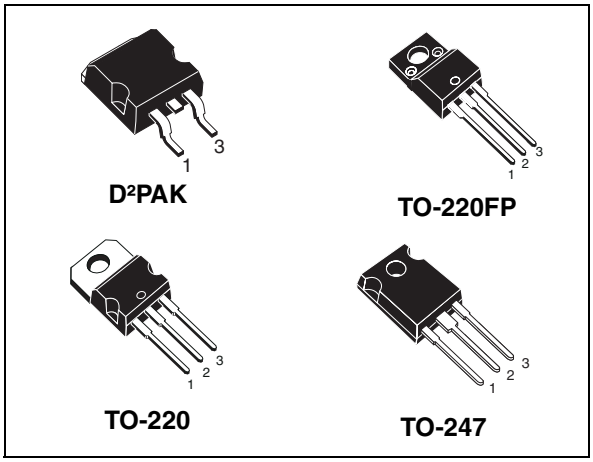
Datasheet — production data

Features

Order codes	V_{DSS}	$R_{DS(on)}$ max	I_D
STB18NM80	800 V	< 0.295 Ω	17 A
STF18NM80	800 V	< 0.295 Ω	17 A (1)
STP18NM80	800 V	< 0.295 Ω	17 A
STW18NM80	800 V	< 0.295 Ω	17 A

1. Limited only by maximum temperature allowed

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance



Application

- Switching applications

Description

These N-channel Power MOSFETs are developed using STMicroelectronics' revolutionary MDmesh™ technology, which associates the multiple drain process with the company's PowerMESH™ horizontal layout. These devices offer extremely low on-resistance, high dv/dt and excellent avalanche characteristics. Utilizing ST's proprietary strip technique, these Power MOSFETs boast an overall dynamic performance which is superior to similar products on the market.

Figure 1. Internal schematic diagram

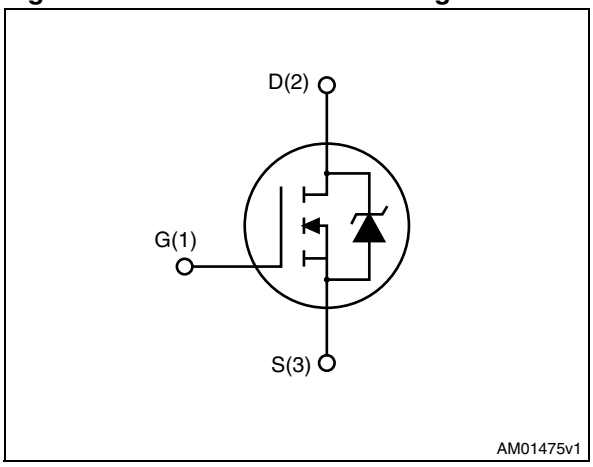


Table 1. Device summary

Order codes	Marking	Package	Packaging
STB18NM80	18NM80	D²PAK	Tape and reel
STF18NM80		TO-220FP	Tube
STP18NM80		TO-220	
STW18NM80		TO-247	

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value				Unit
		TO-220	D²PAK	TO-247	TO-220FP	
V_{DS}	Drain-source voltage	800				V
V_{GS}	Gate-source voltage	± 30				V
I_D	Drain current (continuous) at T_C = 25 °C	17			17 (1)	A
I_D	Drain current (continuous) at T_C = 100 °C	10.71			10.71(1)	A
I_{DM} (2)	Drain current (pulsed)	68			68 (1)	A
P_{TOT}	Total dissipation at T_C = 25 °C	190			40	W
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s;T_C = 25 °C)				2500	V
T_{stg}	Storage temperature	-65 to 150				°C
T_j	Max. operating junction temperature	150				°C

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area

Table 3. Thermal data

Symbol	Parameter	Value				Unit
		TO-220	D²PAK	TO-247	TO-220FP	
$R_{thj-case}$	Thermal resistance junction-case	0.66			3.13	°C/W
$R_{thj-amb}$	Thermal resistance junction-amb	62.5		50	62.5	°C/W
$R_{thj-pcb}$	Thermal resistance junction-pcb		30			°C/W
T_l	Maximum lead temperature for soldering purpose	300				°C

Table 4. Avalanche characteristics

Symbol	Parameter	Max value	Unit
I_{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by Tj max)	4	A
E_{AS}	Single pulse avalanche energy (starting Tj = 25 °C, I_D = I_{AS}, V_{DD} = 50 V)	600	mJ

2 Electrical characteristics

(T_{CASE}= 25 °C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	800			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 800 V, V_{DS} = 800 V,Tc = 125 °C			10 100	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ± 30 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 8.5 A		0.25	0.295	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs}(1)	Forward transconductance	V_{DS} = 15 V, I_D= 8.5 A	-	14	-	S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0	-	2070 210 29	-	pF pF pF
$C_{oss\ eq.}$(2)	Equivalent output capacitance	V_{GS} = 0, V_{DS} = 0 to 640 V	-	316	-	pF
R_G	Gate input resistance	f = 1 MHz Gate DC Bias = 0 Test Signal Level = 20 mV Open Drain	-	4	-	Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 640 V, I_D = 17 A V_{GS} = 10 V	-	70 13 40	-	nC nC nC

1. Pulsed: pulse duration = 300µs, duty cycle 1.5%
2. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 400 V, I_D = 8.5 A, R_G = 4.7 Ω, V_{GS} = 10 V	-	18	-	ns
t_r	Rise time			28		ns
$t_{d(off)}$	Turn-off delay time			96		ns
t_f	Fall time			50		ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		17	A
I_{SDM} (1)	Source-drain current (pulsed)				68	A
V_{SD}(2)	Forward on voltage	I_{SD} = 17 A, V_{GS} = 0	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 17 A, di/dt = 100 A/µs, V_{DD} = 100 V,	-	618		ns
Q_{rr}	Reverse recovery charge			9.6		µC
I_{RRM}	Reverse recovery current			31.2		A
t_{rr}	Reverse recovery time	I_{SD} = 17 A, di/dt = 100 A/µs, V_{DD} = 100 V, Tj=150°C	-	822		ns
Q_{rr}	Reverse recovery charge			13		µC
I_{RRM}	Reverse recovery current			31.8		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220, D²PAK

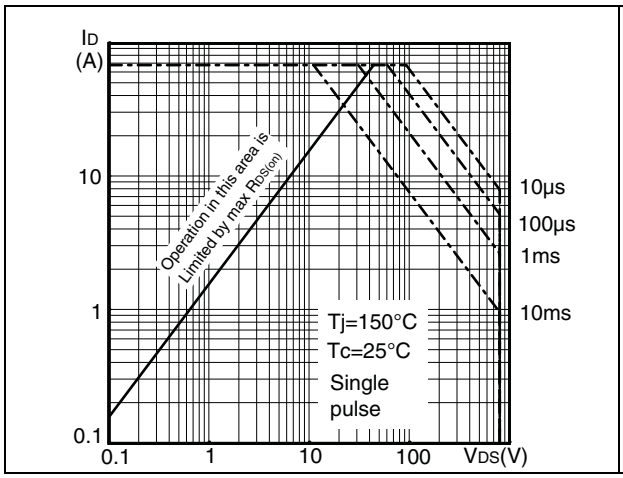


Figure 3. Thermal impedance for TO-220, D²PAK

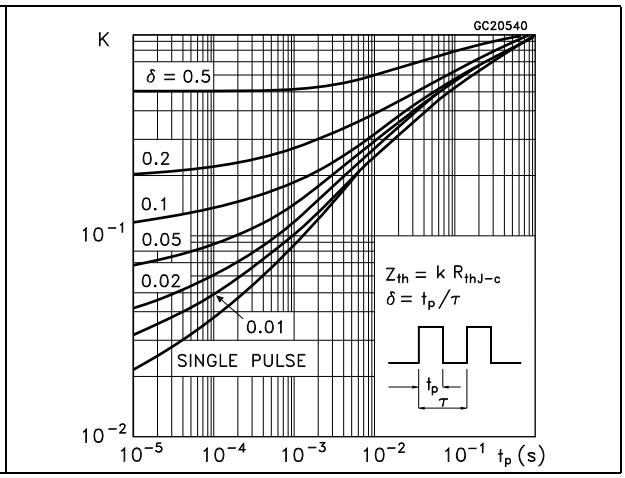


Figure 4. Safe operating area for TO-247

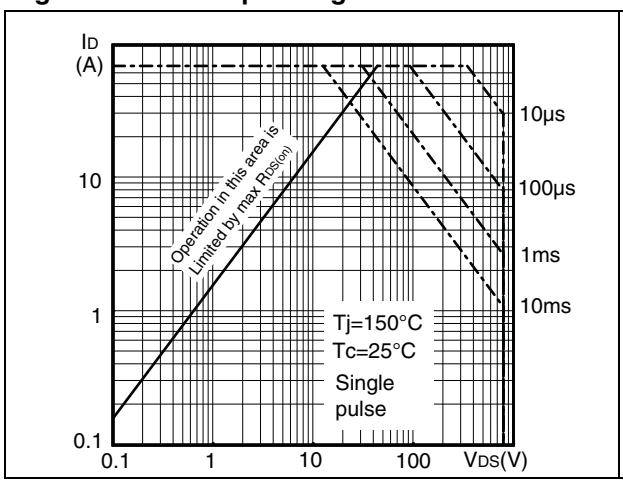


Figure 5. Thermal impedance for TO-247

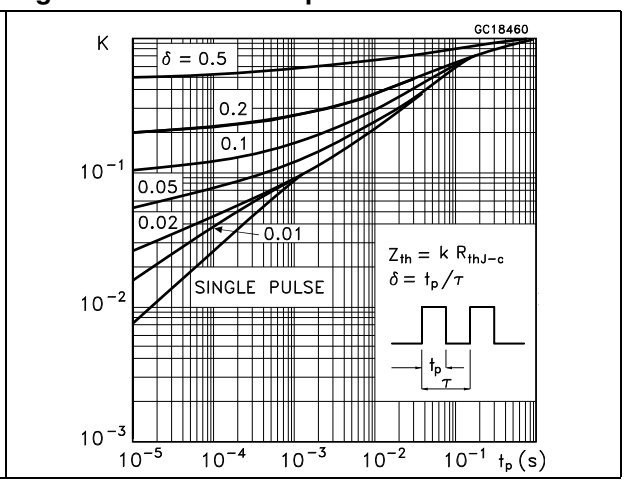


Figure 6. Safe operating area for TO-220FP

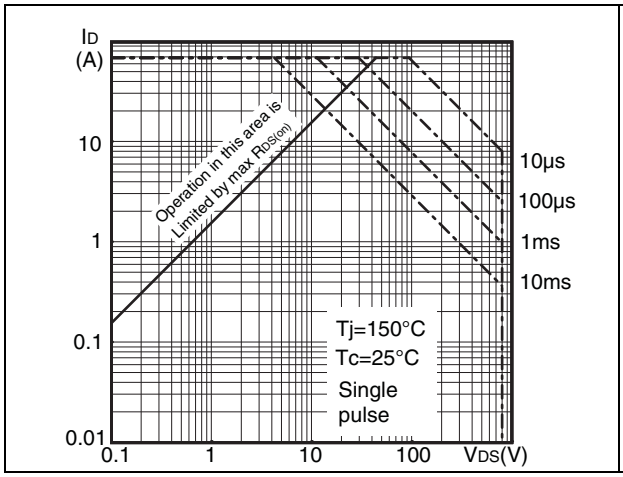


Figure 7. Thermal impedance for TO-220FP