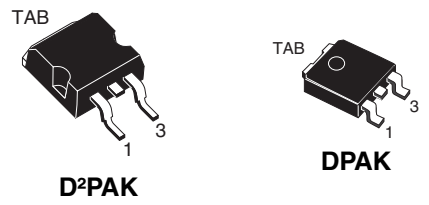
STB16N65M5
STD16N65M5

N-channel 650 V, 0.230 Ω, 12 A MDmesh™ V Power MOSFET in D²PAK, DPAK

Features

Type	V_{DSS} @ T_{Jmax}	$R_{DS(on)}$ max.	I_D
STB16N65M5	710 V	< 0.279 Ω	12 A
STD16N65M5			

- DPAK worldwide best $R_{DS(on)}$
- Higher V_{DSS} rating
- High dv/dt capability
- Excellent switching performance
- Easy to drive
- 100% avalanche tested



Application

- Switching applications

Description

These devices are N-channel MDmesh™ V Power MOSFETs based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

Figure 1. Internal schematic diagram

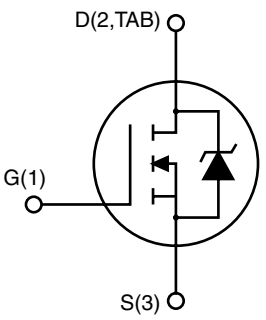


Table 1. Device summary

Order codes	Marking	Package	Packaging
STB16N65M5	16N65M5	D²PAK	Tape and reel
STD16N65M5		DPAK	

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	650	V
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at T_C = 25 °C	12	A
I_D	Drain current (continuous) at T_C = 100 °C	7.3	A
I_{DM} (1)	Drain current (pulsed)	48	A
P_{TOT}	Total dissipation at T_C = 25 °C	90	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	4	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, $I_D = I_{AR}$, V_{DD} = 50 V)	200	mJ
dv/dt (2)	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature	- 55 to 150	°C
T_j	Max. operating junction temperature	150	°C

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 12$ A, di/dt $\leq$ 400 A/µs, V_{DD} = 400 V, $V_{Peak} < V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		DPAK	D²PAK	
$R_{thj\text{-}case}$	Thermal resistance junction-case max	1.38		°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb max	50	30	°C/W

1. When mounted on 1inch² FR-4 board, 2 oz Cu

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage (V_{GS} = 0)	I_D = 1 mA	650			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 650 V V_{DS} = 650 V, T_C=125 °C			1 100	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 25 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 6 A		0.230	0.279	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0	-	1250 30 3	-	pF pF pF
$C_{o(tr)}$(1)	Equivalent capacitance time related	V_{DS} = 0 to 520 V, V_{GS} = 0	-	100	-	pF
$C_{o(er)}$(2)	Equivalent capacitance energy related		-	30	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	2	-	Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 520 V, I_D = 6 A, V_{GS} = 10 V	-	31 8 12	-	nC nC nC

1. $C_{oss\ eq.}$ time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
2. $C_{oss\ eq.}$ energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
t_d (v)	Voltage delay time	V_{DD} = 400 V, I_D = 8 A,		25		ns
t_r (v)	Voltage rise time	R_G = 4.7 Ω, V_{GS} = 10 V	-	7	-	ns
t_f (i)	Current fall time			6		ns
t_c(off)	Crossing time			8		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		12	A
I_{SDM} (1)	Source-drain current (pulsed)				48	A
V_{SD} (2)	Forward on voltage	I_{SD} = 12 A, V_{GS} = 0	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 12 A, di/dt = 100 A/µs		300		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 100 V (see	-	3.5		nC
I_{RRM}	Reverse recovery current			23		A
t_{rr}	Reverse recovery time	I_{SD} = 12 A, di/dt = 100 A/µs		350		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 100 V, T_j = 150 °C	-	4		nC
I_{RRM}	Reverse recovery current			24		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for D²PAK

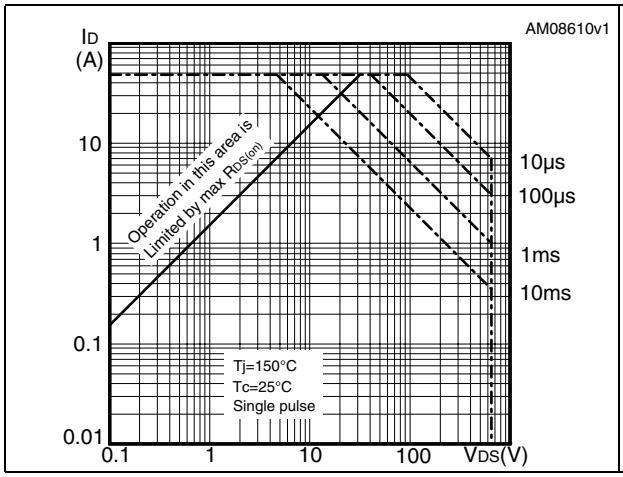


Figure 3. Thermal impedance for D²PAK

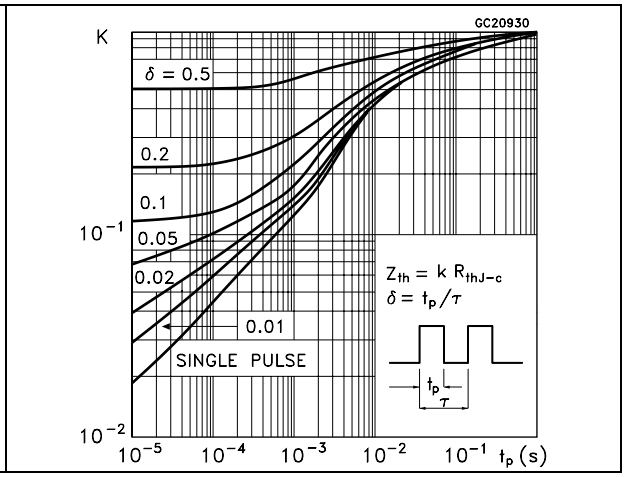


Figure 4. Safe operating area for DPAK

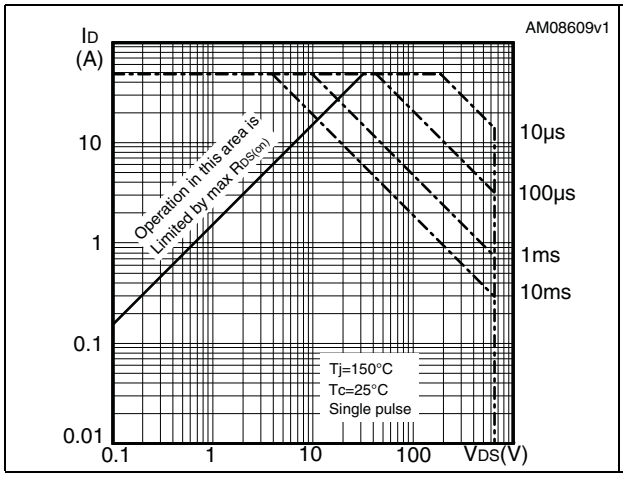


Figure 5. Thermal impedance for DPAK

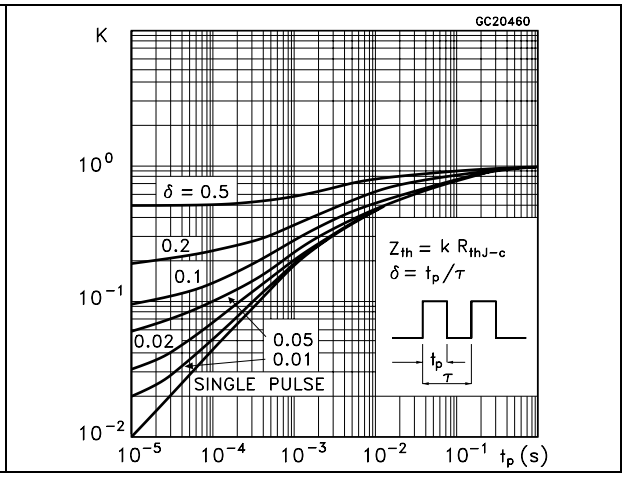


Figure 6. Output characteristics

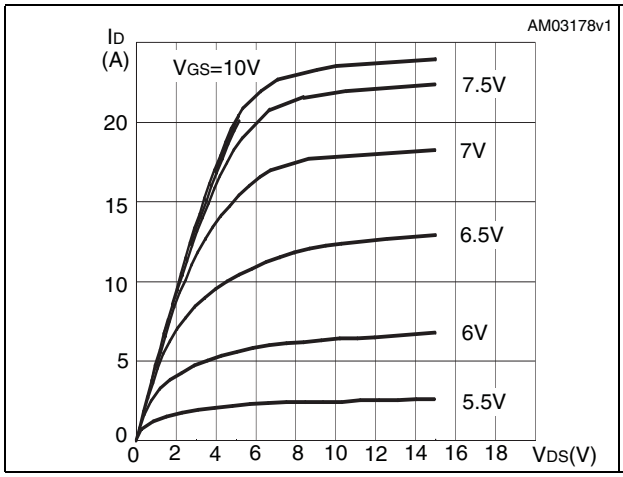


Figure 7. Transfer characteristics