

N-channel 100 V, 4.4 mΩ 120 A TO-220
STripFET™ DeepGATE™ Power MOSFET

Features

Order code	V _{DSS}	R _{DS(on)} max	I _D
STP165N10F4	100 V	< 5.5 mΩ	120 A

- N-channel enhancement mode
- 100% avalanche rated
- Low gate charge
- Very low on-resistance

Application

Switching applications

Description

The STP165N10F4 is an N-channel enhancement mode Power MOSFET built with STripFET™ DeepGATE™ technology with a new gate structure. The product is tailored to minimize on-resistance.

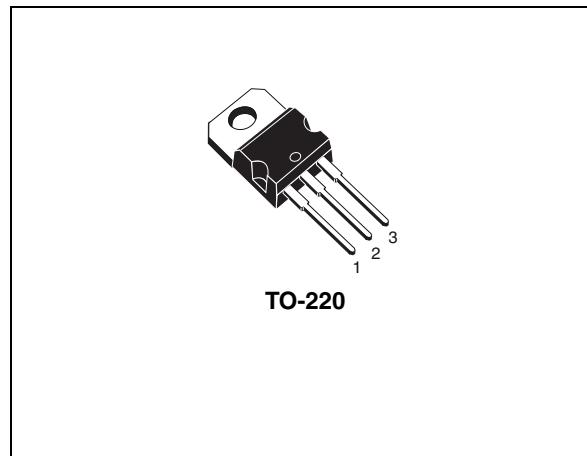
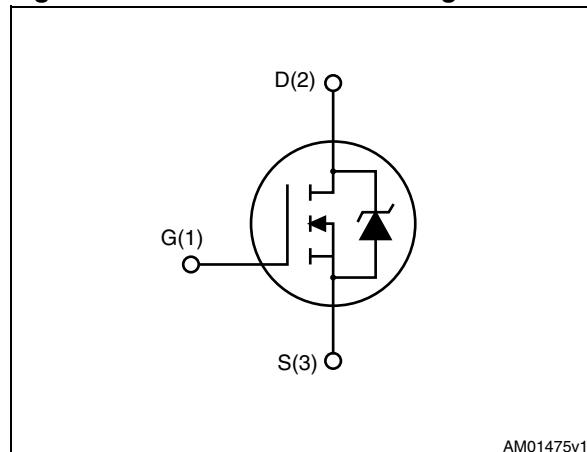


Figure 1. Internal schematic diagram



AM01475v1

Table 1. Device summary

Order code	Marking	Package	Packaging
STP165N10F4	165N10F4	TO-220	Tube

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	100	V
V_{GS}	Gate- source voltage	± 20	V
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$	120	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	110	A
$I_{DM}^{(1)}$	Drain current (pulsed)	480	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	315	W
	Derating factor	2.1	W/ $^\circ\text{C}$
$E_{AS}^{(2)}$	Single pulse avalanche energy	500	mJ
T_{stg}	Storage temperature	- 55 to 150	$^\circ\text{C}$
T_j	Max. operating junction temperature	150	

1. Pulse width limited by safe operating area
2. Starting $T_j = 25^\circ\text{C}$, $I_D = 58\text{ A}$, $V_{DD} = 50\text{ V}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.48	$^\circ\text{C/W}$
R_{thj-a}	Thermal resistance junction-ambient max	62.5	$^\circ\text{C/W}$
T_I	Maximum lead temperature for soldering purpose	315	$^\circ\text{C}$

2 Electrical characteristics

($T_{CASE}=25^\circ\text{C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0$	100			V
I_{DSS}	Zero gate voltage Drain current ($V_{GS} = 0$)	$V_{DS} = \text{max rating}$ $V_{DS} = \text{max rating}, T_C=125^\circ\text{C}$			1 100	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20 \text{ V}$			100	nA
$V_{GS(\text{th})}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	2		4	V
$R_{DS(\text{on})}$	Static drain-source on resistance	$V_{GS} = 10 \text{ V}, I_D = 60 \text{ A}$		4.4	5.5	$\text{m}\Omega$

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance			10750	-	pF
C_{oss}	Output capacitance	$V_{DS} = 25 \text{ V}, f = 1 \text{ MHz}$,	-	939	-	pF
C_{rss}	Reverse transfer capacitance	$V_{GS} = 0$		603	-	pF
Q_g	Total gate charge	$V_{DD} = 50 \text{ V}, I_D = 120 \text{ A}$,	-	192	-	nC
Q_{gs}	Gate-source charge	$V_{GS} = 10 \text{ V}$		48	-	nC
Q_{gd}	Gate-drain charge			62	-	nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	$V_{DD} = 50 \text{ V}$, $I_D = 60 \text{ A}$ $R_G = 4.7 \Omega$ $V_{GS} = 10 \text{ V}$	-	29.6 62	-	ns ns
$t_{d(off)}$ t_f	Turn-off-delay time Fall time	$V_{DD} = 50 \text{ V}$, $I_D = 60 \text{ A}$, $R_G = 4.7 \Omega$ $V_{GS} = 10 \text{ V}$	-	154 106	-	ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		120	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		480	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 120 \text{ A}$, $V_{GS} = 0$	-		1.4	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 120 \text{ A}$, $V_{DD} = 80 \text{ V}$ $di/dt = 100 \text{ A}/\mu\text{s}$, $T_j = 150 \text{ }^\circ\text{C}$ (see)	-	86.8 313 7.2		ns nC A

1. Pulse width limited by safe operating area.

2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

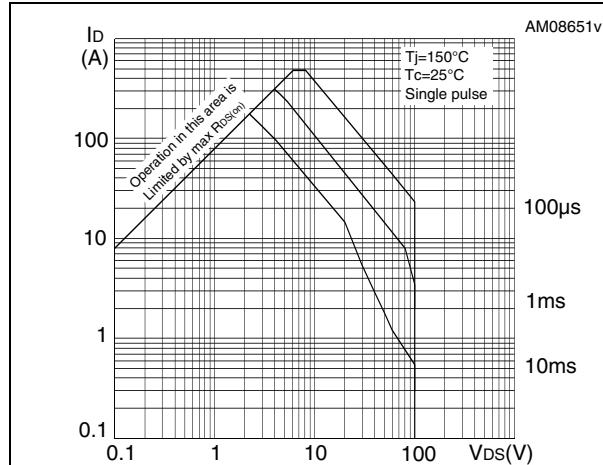


Figure 3. Thermal impedance

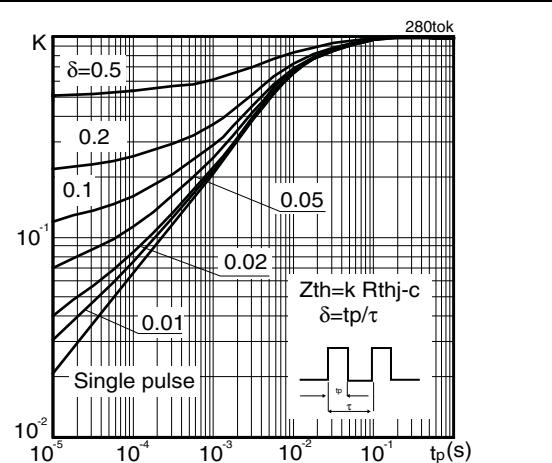


Figure 4. Output characteristics

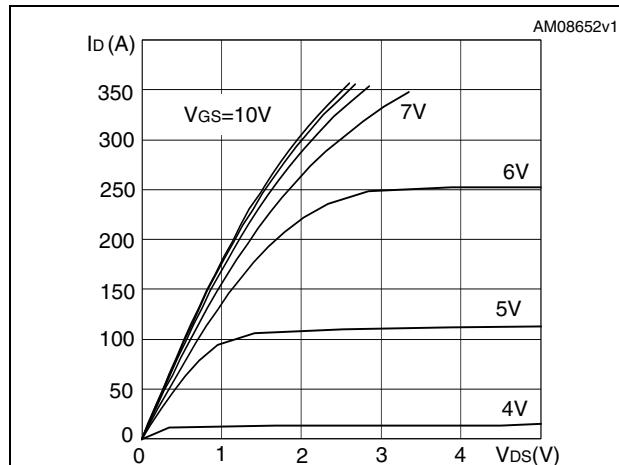


Figure 5. Transfer characteristics

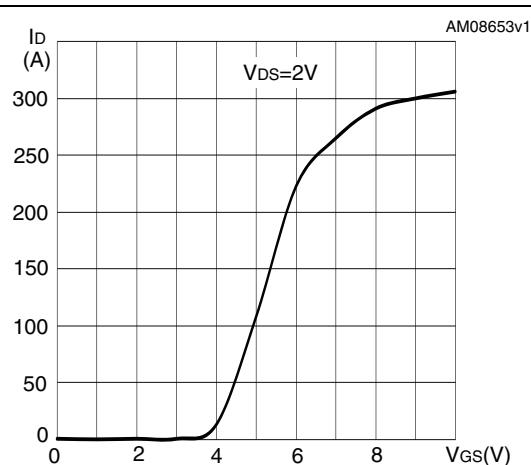
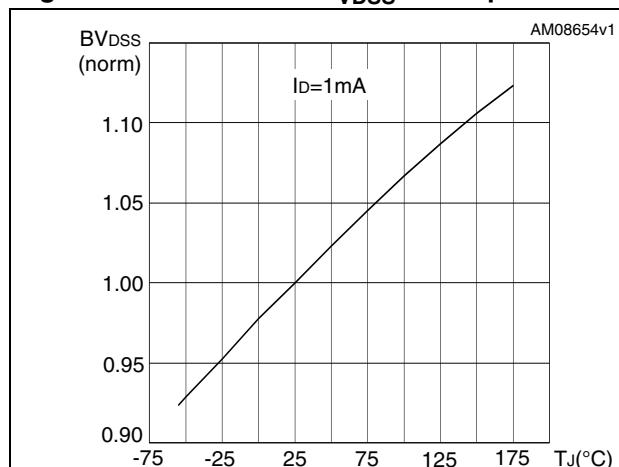
Figure 6. Normalized B_{VDSS} vs temperature

Figure 7. Static drain-source on resistance

