STP150NF04

N-channel 40 V, 0.005 Ω typ., 80 A STripFET™II Power MOSFET in a TO-220 package

Datasheet — production data

Features

Type	V_{DSS}	$R_{DS(on)}$ max	I_D
STP150NF04	40 V	< 0.007 Ω	80 A

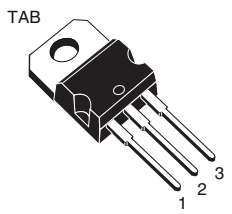
- 100% avalanche tested
- Standard level gate drive

Applications

- Switching applications

Description

This Power MOSFET has been developed using STMicroelectronics' unique STripFET process, which is specifically designed to minimize input capacitance and gate charge. This renders the device suitable for use as primary switch in advanced high-efficiency isolated DC-DC converters for telecom and computer applications, and applications with low gate charge driving requirements.



TO-220

Figure 1. Internal schematic diagram

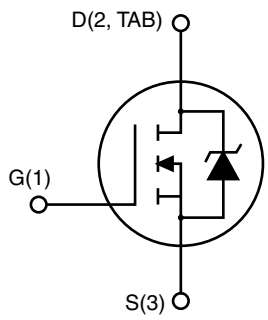


Table 1. Device summary

Order code	Marking	Package	Packaging
STP150NF04	P150NF04	TO-220	Tube

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	40	V
V_{GS}	Gate- source voltage	± 20	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	80	A
I_D (1)	Drain current (continuous) at T_C = 100 °C	80	A
I_{DM} (2)	Drain current (pulsed)	320	A
P_{tot}	Total dissipation at T_C = 25 °C	300	W
	Derating factor	2	W/°C
dv/dt (3)	Peak diode recovery voltage slope	2	V/ns
E_{AS} (4)	Single pulse avalanche energy	0.6	J
T_{stg}	Storage temperature	-55 to 175	°C
T_j	Max. operating junction temperature		

1. Current limited by package
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 80A$, di/dt $\leq$ 300 A/µs, V_{DD}= 80%$V_{(BR)DSS}$
4. Starting Tj = 25 °C, I_D= 40 A, V_{DD}=30 V

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	0.5	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb max	35	°C/W

1. When mounted on 1inch² FR-4 board, 2 oz of Cu

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS} = 0	40			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 40 V V_{DS} = 40 V @ T_j= 125 °C			1 10	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = $V_{GS,}$ I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 40 A		0.005	0.007	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs}(1)	Forward transconductance	V_{DS} = 15 V, I_D = 15 A	-	90	-	S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V, f =1 MHz V_{GS}=0	-	3650 1145 400	-	pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD}=32 V, I_D=80 A, V_{GS}=10 V	-	118 20 45	150	nC nC nC

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD} = 25 V, I_D = 40 A R_G = 4.7 Ω, V_{GS} = 10 V	-	15 150 70 45	-	ns ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		80	A
I_{SDM}(1)	Source-drain current (pulsed)	I_{SD} = 80 A, V_{GS} = 0	-		320	A
V_{SD}(2)	Forward on voltage	I_{SD} = 80 A, V_{GS} = 0	-		1.3	
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD}= 80 A, di/dt=100 A/µs V_{DD} = 25 V, T_j = 150 °C	-	73 170 4.6		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300µs, duty cycle 1.5%