STB14NM50N, STD14NM50N, STF14NM50N, STI14NM50N, STP14NM50N

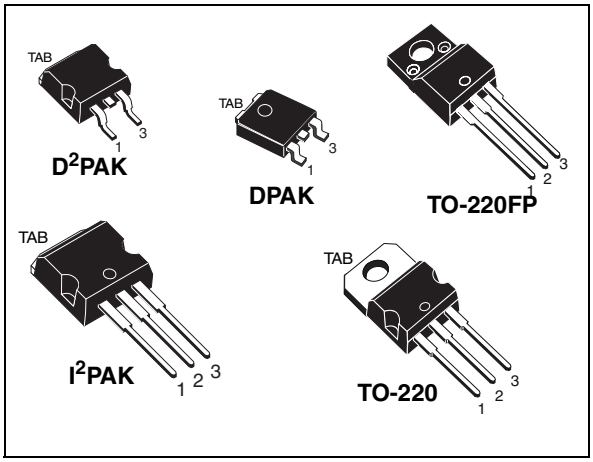
N-channel 500 V, 0.28 Ω typ., 12 A MDmesh™ II Power MOSFET in D²PAK, DPAK, TO-220FP, I²PAK and TO-220 packages

Datasheet — production data

Features

Order codes	V_{DS} @ T_{Jmax}	$R_{DS(on)}$ max	I_D
STB14NM50N STD14NM50N STF14NM50N STI14NM50N STP14NM50N	550 V	0.32 Ω	12 A

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance



Applications

- Switching applications

Description

These devices are N-channel Power MOSFET developed using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

Figure 1. Internal schematic diagram

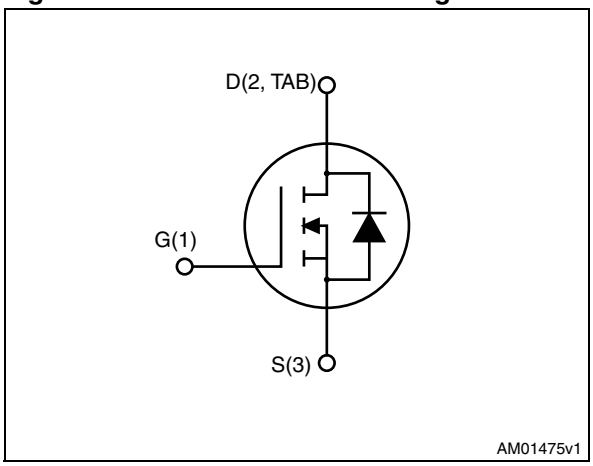


Table 1. Device summary

Order codes	Marking	Package	Packaging
STB14NM50N	14NM50N	D²PAK	Tape and reel
STD14NM50N		DPAK	
STF14NM50N		TO-220FP	Tube
STI14NM50N		I²PAK	
STP14NM50N		TO-220	

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		D^2PAK, DPAK I^2PAK, TO-220	TO-220FP	
V_{DS}	Drain-source voltage	500		V
V_{GS}	Gate-source voltage	± 25		V
I_D	Drain current (continuous) at T_C = 25 °C	12	12 (1)	A
I_D	Drain current (continuous) at T_C = 100 °C	8	8 (1)	A
I_{DM} (2)	Drain current (pulsed)	48	48 (1)	A
P_{TOT}	Total dissipation at T_C = 25 °C	90	25	W
dv/dt (3)	Peak diode recovery voltage slope	15		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; Tc = 25 °C)		2500	V
T_{stg}	Storage temperature	- 55 to 150		°C
T_j	Max. operating junction temperature	150		°C

1. Limited by maximum junction temperature
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 12$ A, di/dt ≤ 400 A/s, V_{DS} peak $\leq V_{(BR)DSS}$, V_{DD} = 80% $V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value					Unit
		D^2PAK	DPAK	TO-220FP	I^2PAK	TO-220	
$R_{thj-case}$	Thermal resistance junction-case max	1.39		5	1.39		°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient max			62.5			°C/W
$R_{thj-pcb}$ (1)	Thermal resistance junction-pcb max	30	50				°C/W

1. When mounted on 1inch² FR-4 board, 2 oz Cu

Table 4. Avalanche data

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	4	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25°C, $I_D = I_{AR}$, V_{DD} = 50 V)	172	mJ

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	500			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 620 V V_{DS} = 620 V, T_C=125 °C			1 100	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 25 V			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 6 A		0.28	0.32	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0	-	816 60 3	-	pF pF pF
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{DS} = 0 to 50 V, V_{GS} = 0	-	307.5	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	4.5	-	Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} =400 V, I_D =12 A, V_{GS} =10 V (see	-	27 4.6 15	-	nC nC nC

1. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off-delay time Fall time	V_{DD} = 400 V, I_D = 12 A, R_G =4.7 Ω, V_{GS} = 10 V	-	10.2 16 42 22	-	ns ns ns ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)		-		12 48	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 12 A, V_{GS} = 0	-		1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 12 A, di/dt = 100 V/ns, V_{DD} = 400 V	-	252 2.8 22		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 12 A, di/dt = 100 V/ns, V_{DD} = 400 V, T_J = 150 °C	-	300 3.3 22.2		ns µC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%