STP14NK60Z - STP14NK60ZFP
STB14NK60Z/-1 - STW14NK60Z

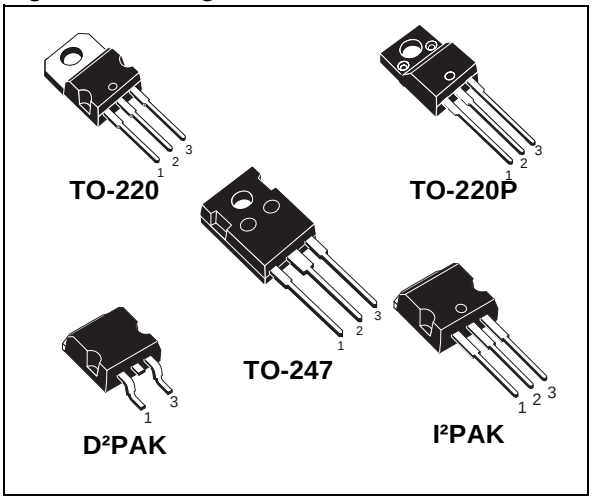
N-CHANNEL 600V - 0.45Ω - 13.5A TO-220/FP-D²/I²PAK-TO-247
Zener-Protected SuperMESH™ MOSFET

Table 1: General Features

TYPE	V_{DSS}	$R_{DS(on)}$	I_D	Pw
STP14NK60Z	600 V	< 0.5 Ω	13.5 A	160 W
STP14NK60ZFP	600 V	< 0.5 Ω	13.5 A	40 W
STB14NK60Z	600 V	< 0.5 Ω	13.5 A	160 W
STB14NK60Z-1	600 V	< 0.5 Ω	13.5 A	160 W
STW14NK60Z	600 V	< 0.5 Ω	13.5 A	160 W

- TYPICAL $R_{DS}(on)$ = 0.45 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- GATE CHARGE MINIMIZED
- VERY LOW INTRINSIC CAPACITANCES
- VERY GOOD MANUFACTURING REPEATIBILITY

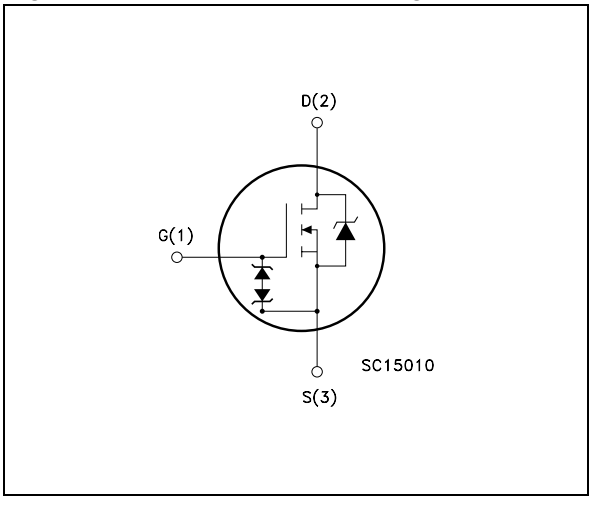
Figure 1: Package



DESCRIPTION

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOS-FETs including revolutionary MDmesh™ products.

Figure 2: Internal Schematic Diagram



APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- IDEAL FOR OFF-LINE POWER SUPPLIES, ADAPTORS AND PFC
- LIGHTING

Table 2: Order Codes

Part Number	Marking	Package	Packaging
STP14NK60Z	P14NK60Z	TO-220	TUBE
STP14NK60ZFP	P14NK60ZFP	TO-220FP	TUBE
STB14NK60ZT4	B14NK60Z	D²PAK	TAPE & REEL
STB14NK60Z-1	B14NK60Z	I²PAK	TUBE
STW14NK60Z	W14NK60Z	TO-247	TUBE

Table 3: Absolute Maximum ratings

Symbol	Parameter	Value		Unit
		TO-220/D²PAK/I²PAK TO-247	TO-220FP	
V_{DS}	Drain-source Voltage (V_{GS} = 0)	600		V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	600		V
V_{GS}	Gate-source Voltage	± 30		V
I_D	Drain Current (continuous) at T_C = 25°C	13.5	13.5 (*)	A
I_D	Drain Current (continuous) at T_C = 100°C	8.5	8.5 (*)	A
I_{DM} (•)	Drain Current (pulsed)	54	54 (*)	A
P_{TOT}	Total Dissipation at T_C = 25°C	160	40	W
	Derating Factor	1.28	0.32	W/°C
$V_{ESD(G-S)}$	Gate source ESD (HBM-C= 100pF, R= 1.5kΩ)	4000		V
dv/dt (1)	Peak Diode Recovery voltage slope	4.5		V/ns
V_{ISO}	Insulation Winthstand Voltage (DC)	--	2500	V
T_j T_{stg}	Operating Junction Temperature Storage Temperature	-55 to 150		°C

(•) Pulse width limited by safe operating area
(1) $I_{SD} \le 13.5A$, $di/dt \le 200$ A/µs, $V_{DD} \le V_{(BR)DSS}$, $T_j \le T_{JMAX}$.
(*) Limited only by maximum temperature allowed

Table 4: Thermal Data

		TO-220/D²PAK/I²PAK TO-247	TO-220FP	Unit
Rthj-case	Thermal Resistance Junction-case Max	0.78	3.1	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	62.5	50	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose	300		°C

Table 5: Avalanche Characteristics

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	12	A
E_{AS}	Single Pulse Avalanche Energy (starting T_j = 25 °C, $I_D = I_{AR}$, V_{DD} = 50 V)	300	mJ

Table 6: Gate-Source Zener Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate source Breakdown Voltage	I_{gs}= ± 1 mA (Open Drain)	30			V

PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

ELECTRICAL CHARACTERISTICS (T_{CASE} =25°C UNLESS OTHERWISE SPECIFIED)

Table 7: On/Off

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 1mA, V_{GS} = 0	600			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating, T_C = 125 °C			1 50	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 30V			±10	µA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	3.75	4.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10V, I_D = 6 A		0.45	0.5	Ω

Table 8: Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	V_{DS} = 15 V, I_D= 6 A		11		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		2220 240 57		pF pF pF
$C_{oss\ eq.}$ (3)	Equivalent Output Capacitance	V_{GS} = 0V, V_{DS} = 0V to 480V		122		pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on Delay Time Rise Time Turn-off Delay Time Fall Time	V_{DD} = 300 V, I_D = 6 A, R_G= 4.7 Ω, V_{GS} = 10 V (Resistive Load see, Figure 21)		26 18 62 13		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD} = 480V, I_D = 12 A, V_{GS} = 10V (see, Figure 24)		75 13.2 38.6		nC nC nC

Table 9: Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (2)	Source-drain Current Source-drain Current (pulsed)				12 48	A A
V_{SD} (1)	Forward On Voltage	I_{SD} = 12 A, V_{GS} = 0			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 12 A, di/dt = 100 A/µs V_{DD} = 50 V, T_j = 25°C (see test circuit, Figure 22)		490 4.7 19.3		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 12 A, di/dt = 100 A/µs V_{DD} = 50 V, T_j = 150°C (see test circuit, Figure 22)		664 6.8 20.5		ns µC A

(1) Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
(2) Pulse width limited by safe operating area.
(3) $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as Coss when VDS increases from 0 to 80% VDSS

Figure 3: .Safe Operating Area For TO-220/ D²PAK/I²PAK

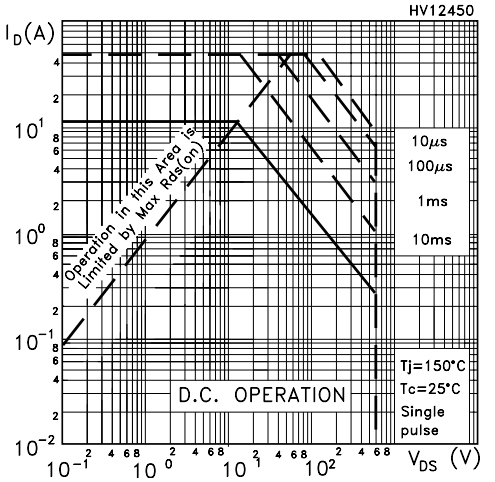


Figure 4: Safe Operating Area For TO-220FP

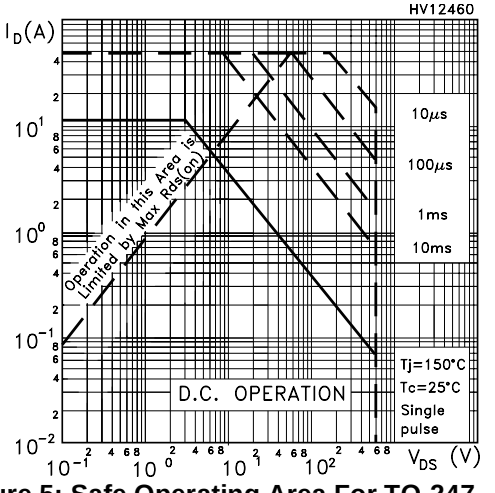


Figure 5: Safe Operating Area For TO-247

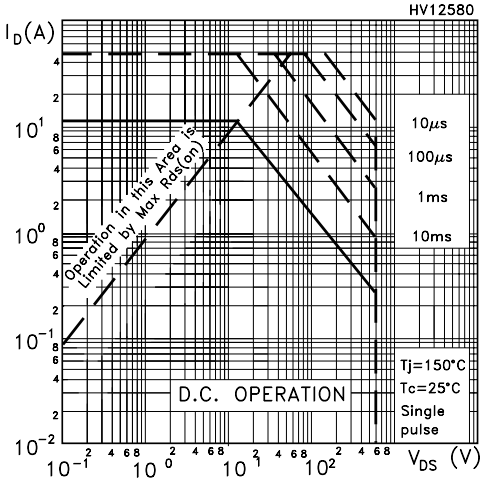


Figure 6: Thermal Impedance For TO-220/ D²PAK/I²PAK

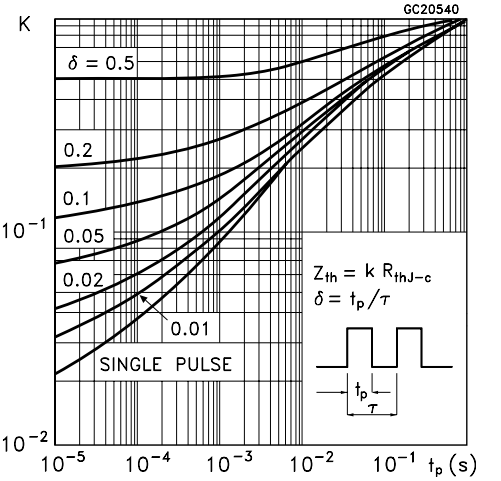


Figure 7: Thermal Impedance For TO-220FP

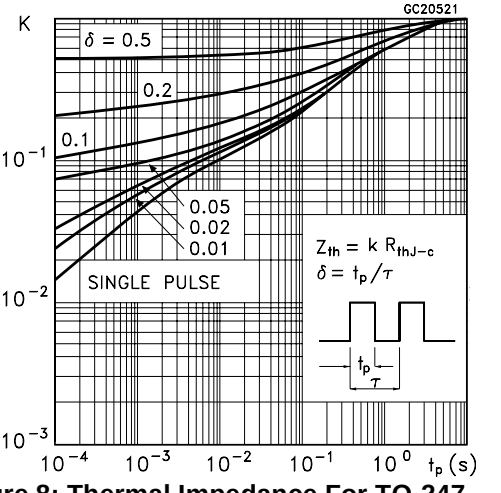


Figure 8: Thermal Impedance For TO-247