STP140NF75
STB140NF75 - STB140NF75-1

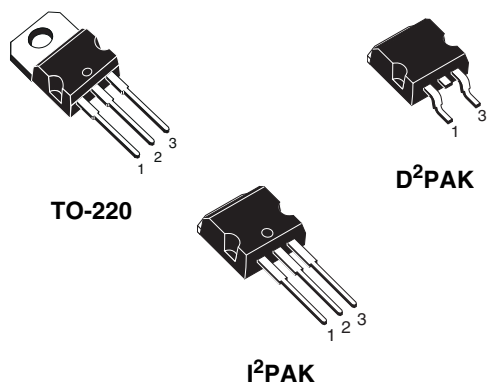
N-channel 75V - 0.0065Ω - 120A - $D^2PAK/I^2/TO-220$
STripFET™ III Power MOSFET

General features

Type	V_{DSS}	$R_{DS(on)}$	I_D
STB140NF75	75V	<0.0075Ω	120A(1)
STB140NF75-1	75V	<0.0075Ω	120A(1)
STP140NF75	75V	<0.0075Ω	120A(1)

1. Current limited by package

- 100% avalanche tested



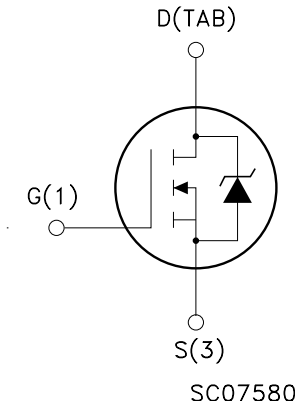
Description

This Power MOSFET is the latest development of STMicroelectronis unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

Applications

- Switching application

Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STB140NF75T4	B140NF75	D^2PAK	Tape & reel
STB140NF75-1	B140NF75	I^2PAK	Tube
STP140NF75	P140NF75	TO-220	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	75	V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 kΩ)	75	V
V_{GS}	Gate- source voltage	± 20	V
I_D(1)	Drain current (continuous) at T_C = 25°C	120	A
I_D(1)	Drain current (continuous) at T_C = 100°C	100	A
I_{DM}(2)	Drain current (pulsed)	480	A
P_{tot}	Total dissipation at T_C = 25°C	310	W
	Derating Factor	2.08	W/°C
dv/dt (3)	Peak diode recovery voltage slope	10	V/ns
E_{AS} (4)	Single pulse avalanche energy	750	mJ
T_{stg}	Storage temperature	-55 to 175	°C
T_j	Max. operating junction temperature		

1. Value limited by wire bonding
2. Pulse width limited by safe operating area.
3. $I_{SD} \leq 120A$, di/dt ≤400A/µs, $V_{DD} \leq V_{(BR)DSS}$, $Tj \leq T_{JMAX}$
4. Starting T_j = 25 °C, I_D = 60A, V_{DD} = 30V

Table 2. Thermal data

Rthj-case	Thermal resistance junction-case max	0.48	°C/W
Rthj-amb	Thermal resistance junction-ambient max	62.5	°C/W
T_J	Maximum lead temperature for soldering purpose(1)	300	°C

1. for 10 sec. 1.6mm from case

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250µA, V_{GS} =0	75			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = max ratings V_{DS} = max ratings, T_C = 125°C			1 10	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250µA	2		4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10V, I_D = 70A		0.0065	0.0075	Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 15V, I_D = 70A		160		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25V, f = 1MHz, V_{GS} = 0		5000 960 310		pF pF pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD} = 38V, I_D = 70A R_G = 4.7Ω V_{GS} = 10V		30 140 130 90		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 60V, I_D = 120A, V_{GS} = 10V		160 28 70	218	nC nC nC

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.

Table 5. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)				120 480	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 120A, V_{GS} = 0			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 120A, di/dt = 100A/µs, V_{DD} = 35V, T_j = 150°C		115 450 8		ns nC A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %