

N-CHANNEL 55V - 0.0065 Ω - 80A TO-220/D²PAK STripFET™ II POWER MOSFET

Table 1: General Features

TYPE	V _{DSS}	R _{DS(on)}	I _D
STB140NF55	55 V	< 0.008 Ω	80 A
STP140NF55	55 V	< 0.008 Ω	80 A

- TYPICAL R_{DS(on)} = 0.0065 Ω

DESCRIPTION

This Power Mosfet is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

APPLICATIONS

- MOTOR CONTROL
- HIGH CURRENT, SWITCHING APPLICATIONS
- AUTOMOTIVE ENVIRONMENT

Figure 1: Package

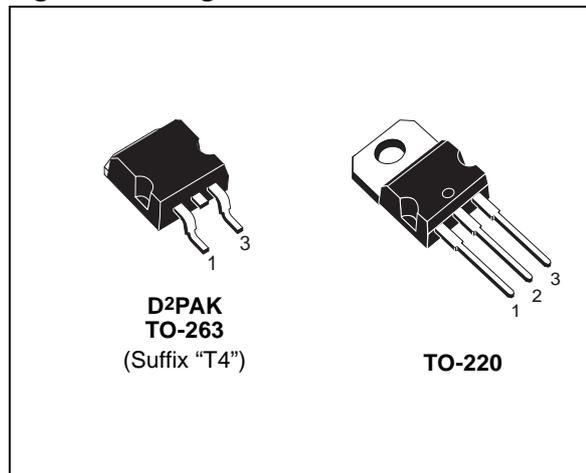


Figure 2: Internal Schematic Diagram

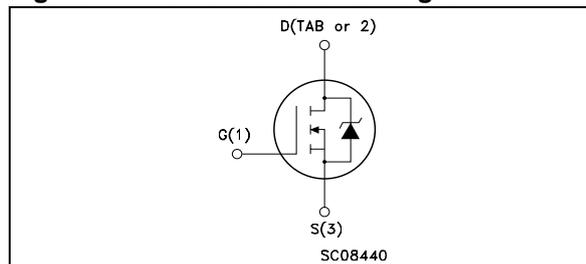


Table 2: Order Codes

Part Number	MARKING	PACKAGE	PACKAGING
STB140NF55T4	B140NF55	D ² PAK	TAPE & REEL
STP140NF55	P140NF55	TO-220	TUBE

Table 3: ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	55	V
V _{GS}	Gate- source Voltage	± 20	V
I _D	Drain Current (continuous) at T _C = 25°C	80	A
I _D	Drain Current (continuous) at T _C = 100°C	80	A
I _{DM} (●)	Drain Current (pulsed)	320	A
P _{tot}	Total Dissipation at T _C = 25°C	300	W
	Derating Factor	2	W/°C
dv/dt ⁽¹⁾	Peak Diode Recovery voltage slope	10	V/ns
E _{AS} (2)	Single Pulse Avalanche Energy	1.3	mJ
T _{stg}	Storage Temperature	-55 to 175	°C
T _j	Operating Junction Temperature		

(●) Pulse width limited by safe operating area.

(**) Current Limited by Package

(1) I_{SD} ≤ 80A, di/dt ≤ 300A/μs, V_{DD} ≤ V_{(BR)DSS}, T_j ≤ T_{JMAX}

(2) Starting T_j = 25 °C, I_D = 40A, V_{DD} = 30V

STB140NF55 STP140NF55

Table 4: THERMAL DATA

Rthj-case	Thermal Resistance Junction-case	Max	0.5	°C/W
Rthj-amb	Thermal Resistance Junction-ambient	Max	62.5	°C/W
T _l	Maximum Lead Temperature For Soldering Purpose		300	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

Table 5: OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0	55			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating T _C = 125°C			1 10	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 20 V			±100	nA

Table 6: ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} I _D = 250 μA	2	3	4	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10 V I _D = 40 A		0.0065	0.008	Ω

Table 7: DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (*)	Forward Transconductance	V _{DS} = 25 V I _D = 40 A		100		S
C _{iss}	Input Capacitance	V _{DS} = 25V f = 1 MHz V _{GS} = 0		5300		pF
C _{oss}	Output Capacitance			1000		pF
C _{rss}	Reverse Transfer Capacitance			290		pF

ELECTRICAL CHARACTERISTICS (continued)

Table 8: SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	$V_{DD} = 27.5\text{ V}$ $I_D = 40\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (Resistive Load, Figure 3)		30 150		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 44\text{ V}$ $I_D = 80\text{ A}$ $V_{GS} = 10\text{ V}$		142 27 55		nC nC nC

Table 9: SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	$V_{DD} = 27.5\text{ V}$ $I_D = 40\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (Resistive Load, Figure 3)		125 45		ns ns

Table 10: SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM} (\bullet)$	Source-drain Current Source-drain Current (pulsed)				80 320	A A
$V_{SD} (*)$	Forward On Voltage	$I_{SD} = 80\text{ A}$ $V_{GS} = 0$			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 80\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 20\text{ V}$ $T_j = 150^\circ\text{C}$ (see test circuit, Figure 5)		90 275 6.5		ns μC A

(*)Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.
 (•)Pulse width limited by safe operating area.

Figure 3: Safe Operating Area

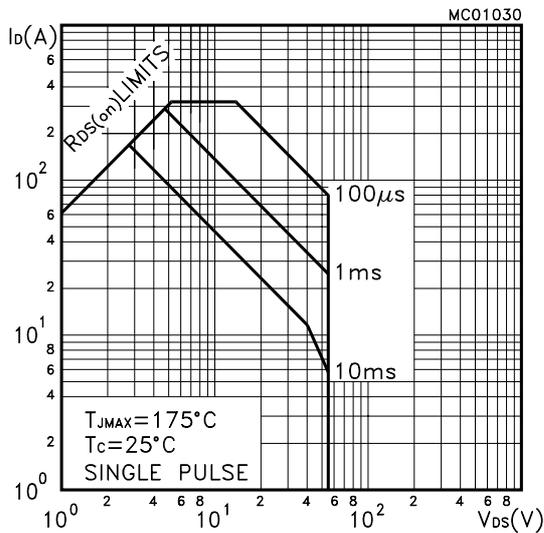


Figure 4: Thermal Impedance

