STD13NM60ND, STF13NM60ND, STP13NM60ND

N-channel 600 V, 0.32 Ω typ., 11 A, FDmesh™ II Power MOSFET (with fast diode) in DPAK, TO-220FP and TO-220 packages

Datasheet — production data

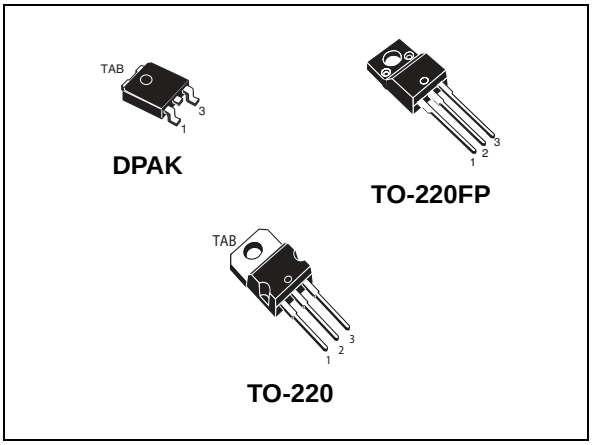
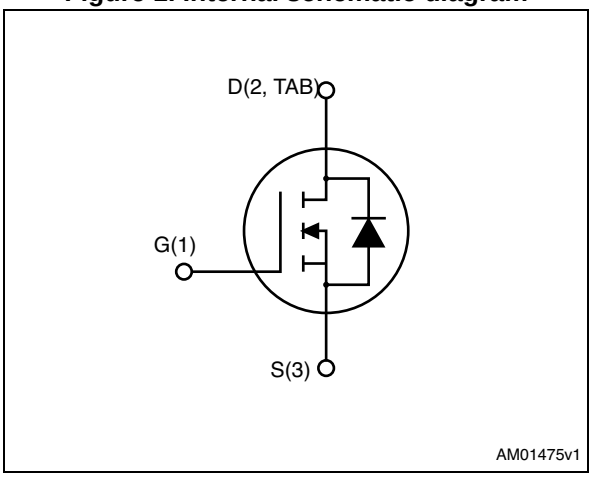


Figure 1. Internal schematic diagram



Features

Order codes	V_{DS} @ T_{Jmax}	$R_{DS(on)}$ max	I_D
STD13NM60ND	650 V	0.38 Ω	11 A
STF13NM60ND			
STP13NM60ND			

- The worldwide best $R_{DS(on)}$* area among fast recovery diode devices
- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance
- Extremely high dv/dt and avalanche capabilities

Applications

- Switching applications

Description

These FDmesh™ II Power MOSFETs with intrinsic fast-recovery body diode are produced using the second generation of MDmesh™ technology. Utilizing a new strip-layout vertical structure, these revolutionary devices feature extremely low on-resistance and superior switching performance. They are ideal for bridge topologies and ZVS phase-shift converters.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STD13NM60ND	13NM60ND	DPAK	Tape and reel
STF13NM60ND		TO-220FP	Tube
STP13NM60ND		TO-220	

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		DPAK, TO-220	TO-220FP	
V_{DS}	Drain-source voltage	600		V
V_{GS}	Gate-source voltage	± 25		V
I_D	Drain current (continuous) at T_C = 25°C	11	11 (1)	A
I_D	Drain current (continuous) at T_C = 100°C	6.93	6.93(1)	A
I_{DM} (2)	Drain current (pulsed)	44	44 (1)	A
P_{TOT}	Total dissipation at T_C = 25°C	109	25	W
dv/dt (3)	Peak diode recovery voltage slope	40		V/ns
dv/dt (4)	MOSFET dv/dt ruggedness	40		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1s;T_C=25°C)		2500	V
T_{stg}	Storage temperature	-55 to 150		°C
T_j	Max. operating junction temperature	150		°C

1. Limited by maximum junction temperature
2. Pulse width limited by safe operating area
3. $I_{SD} \leq$ 11 A, di/dt $\leq$ 400 A/µs, V_{DD} = 80% $V_{(BR)DSS}$, $V_{DS(peak)} \leq V_{(BR)DSS}$
4. $V_{DS} \leq$ 480 V

Table 3. Thermal data

Symbol	Parameter	Value			Unit
		DPAK	TO-220FP	TO-220	
$R_{thj\text{-}case}$	Thermal resistance junction-case max	1.15	5	1.15	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-amb max		62.5		°C/W
$R_{thj\text{-}pcb}$(1)	Thermal resistance junction-pcb max	50			°C/W

1. When mounted on 1inch² FR-4 board, 2 oz Cu

Table 4. Avalanche characteristics

Symbol	Parameter	Max value	Unit
I_{AS}	Avalanche current, repetitive or not-repetitive(1)	3	A
E_{AS}	Single pulse avalanche energy (2)	162	mJ

1. Pulse width limited by Tj max
2. starting Tj= 25 °C, I_D=I_{AS}, V_{DD}= 50 V

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS}= 0	600			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 600 V V_{DS} = 600 V, T_C=125 °C			1 100	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS}= 10 V, I_D= 5.5 A		0.32	0.38	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 50 V, f =1 MHz, V_{GS} = 0	-	845	-	pF
C_{oss}	Output capacitance		-	47	-	pF
C_{rss}	Reverse transfer capacitance		-	2.5	-	pF
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{GS} = 0, V_{DS} = 0V to 480 V	-	121	-	pF
Rg	Gate input resistance	f=1 MHz Gate DC Bias=0 Test signal level=20 mV open drain	-	4.3	-	Ω
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 11 A V_{GS} = 10 V	-	24.5	-	nC
Q_{gs}	Gate-source charge		-	4.8	-	nC
Q_{gd}	Gate-drain charge		-	17	-	nC

1. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 5.5 A, R_G = 4.7 Ω, V_{GS} = 10 V	-	46.5	-	ns
t_r	Rise time		-	10	-	ns
$t_{d(off)}$	Turn-off delay time		-	9.6	-	ns
t_f	Fall time		-	15.4	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
I_{SD}	Source-drain current		-		11	A
I_{SDM} (1)	Source-drain current (pulsed)		-		44	A
V_{SD}(2)	Forward on voltage	I_{SD} = 11 A, V_{GS}=0	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} =11 A, di/dt =100 A/µs, V_{DD} = 100 V	-	150		ns
Q_{rr}	Reverse recovery charge		-	755		nC
I_{RRM}	Reverse recovery current		-	12		A
t_{rr}	Reverse recovery time	V_{DD} = 100 V di/dt =100 A/µs, I_{SD} = 11 A Tj = 150 °C (see	-	187		ns
Q_{rr}	Reverse recovery charge		-	1271		nC
I_{RRM}	Reverse recovery current		-	13.6		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for DPAK

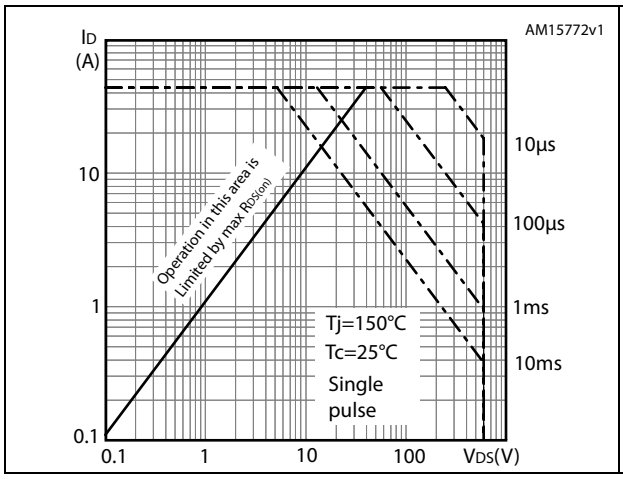


Figure 3. Thermal impedance for DPAK

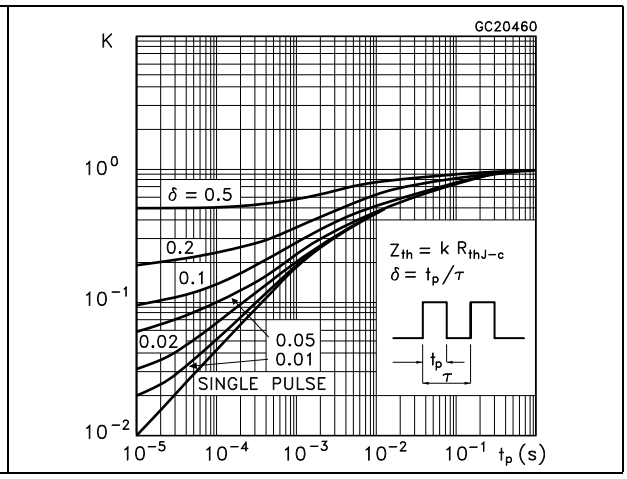


Figure 4. Safe operating area for TO-220FP

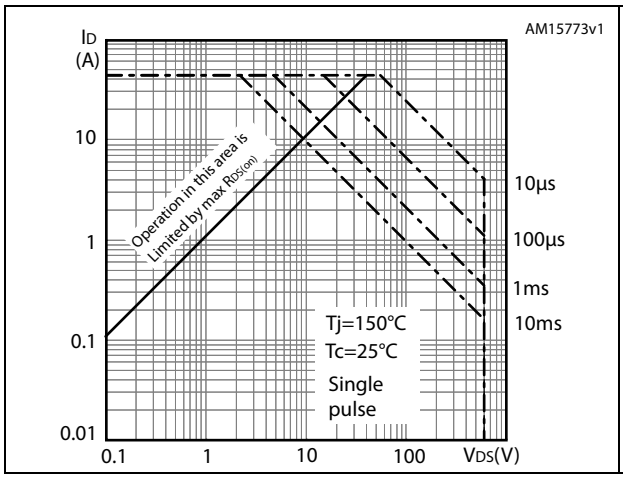


Figure 5. Thermal impedance for TO-220FP

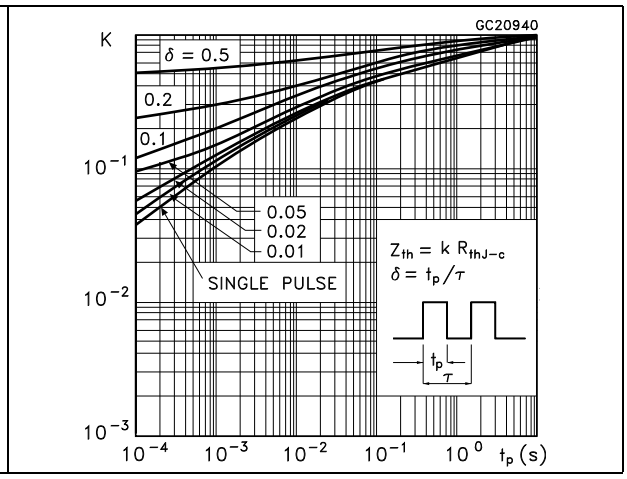


Figure 6. Safe operating area for TO-220

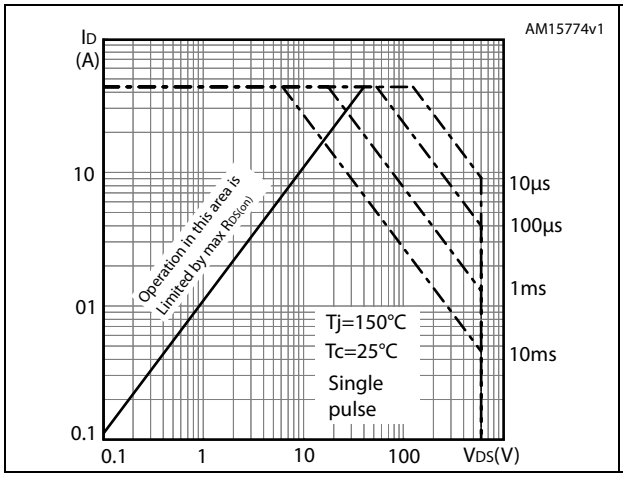


Figure 7. Thermal impedance for TO-220