

STB13NM50N/-1 - STF13NM50N STP13NM50N - STW13NM50N

N-channel 500V - 0.250Ω - 12A - TO-220/FP - TO-247-I²/D²PAK
Second generation MDmesh™ Power MOSFET

Features

Type	V _{DSS} (@T _{jmax})	R _{DS(on)}	I _D
STB13NM50N	550V	<0.32Ω	12A
STB13NM50N-1	550V	<0.32Ω	12A
STF13NM50N	550V	<0.32Ω	12A ⁽¹⁾
STP13NM50N	550V	<0.32Ω	12A
STW13NM50N	550V	<0.32Ω	12A

1. Limited only by maximum temperature allowed

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Description

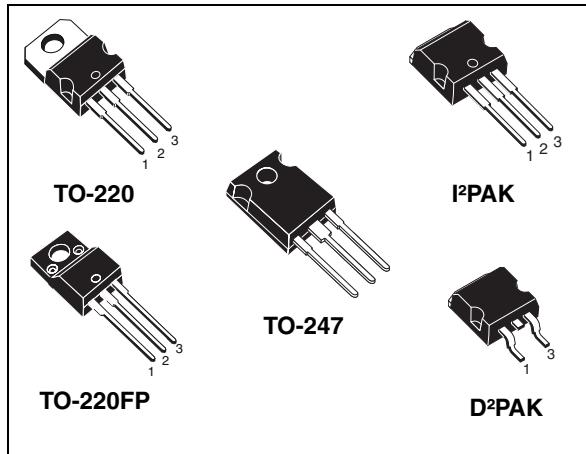
This product is realized with the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a new vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters

Application

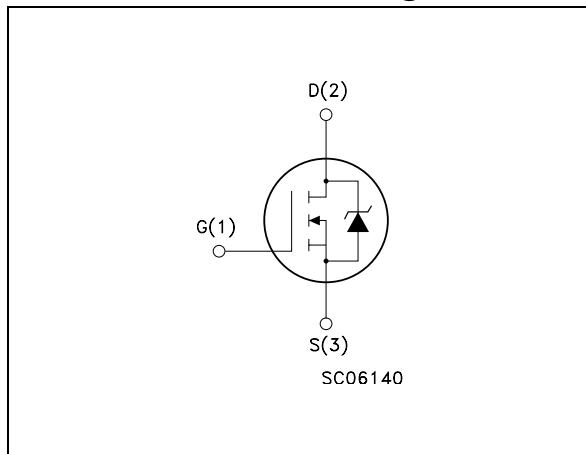
- Switching application

Order codes

Part number	Marking	Package	Packaging
STB13NM50N-1	B13NM50N	I ² PAK	Tube
STB13NM50N	B13NM50N	D ² PAK	Tape & reel
STP13NM50N	P13NM50N	TO-220	Tube
STF13NM50N	F13NM50N	TO-220FP	Tube
STW13NM50N	W13NM50N	TO-247	Tube



Internal schematic diagram



1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220/TO-247 D ² PAK/I ² PAK	TO-220FP	
V _{DS}	Drain-source voltage (V _{GS} =0)	500		V
V _{GS}	Gate-source voltage	± 25		V
I _D	Drain current (continuous) at T _C = 25°C	12	12 ⁽¹⁾	A
I _D	Drain current (continuous) at T _C = 100°C	6	6 ⁽¹⁾	A
I _{DM} ⁽²⁾	Drain current (pulsed)	48	48 ⁽¹⁾	A
P _{TOT}	Total dissipation at T _C = 25°C	100	25	W
dv/dt ⁽³⁾	Peak diode recovery voltage slope	15		V/ns
V _{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1s;T _C =25°C)	--	2500	V
T _j T _{stg}	Operating junction temperature Storage temperature	-55 to 150		°C

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. I_{SD} ≤ 12A, di/dt ≤ 400A/μs, V_{DD} = 80% V_{(BR)DSS}

Table 2. Thermal data

Symbol	Parameter	Value		Unit
		TO-220/TO-247 D ² PAK/I ² PAK	TO-220FP	
R _{thj-case}	Thermal resistance junction-case max	1.25	5	°C/W
R _{thj-amb}	Thermal resistance junction-amb max	62.5		°C/W
T _L	Maximum lead temperature for soldering purpose	300		°C

Table 3. Avalanche characteristics

Symbol	Parameter	Max value	Unit
I _{AS}	Avalanche current, repetitive or non-repetitive (pulse width limited by T _j max)	3.5	A
E _{AS}	Single pulse avalanche energy (starting T _j =25°C, I _D =I _{AS} , V _{DD} = 50V)	200	mJ

2 Electrical characteristics

($T_{CASE}=25^{\circ}\text{C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{mA}, V_{GS} = 0$	500			V
$dv/dt^{(1)}$	Drain-source voltage slope	$V_{DD}=400\text{V}, I_D=12\text{A}, V_{GS}=10\text{V}$		30		V/ns
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}, V_{DS} = \text{Max rating}, T_c=125^{\circ}\text{C}$			1 100	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{V}$			100	nA
$V_{GS(\text{th})}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	2	3	4	V
$R_{DS(\text{on})}$	Static drain-source on resistance	$V_{GS} = 10\text{V}, I_D = 6\text{A}$		0.25	0.32	Ω

1. Characteristics value at turn off on inductive load

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15\text{V}, I_D = 6\text{A}$		8		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 50\text{V}, f = 1\text{MHz}, V_{GS} = 0$		960 50 5		pF pF pF
$C_{oss \text{ eq.}}^{(2)}$	Equivalent output capacitance	$V_{GS} = 0, V_{DS} = 0\text{V to } 480\text{V}$		110		pF
R_g	Gate input resistance	$f = 1\text{MHz}$ Gate DC Bias = 0 test signal level = 20mV open drain		5		Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 400\text{V}, I_D = 12\text{A}$ $V_{GS} = 10\text{V}$		30 5 15		nC nC nC

1. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2. $C_{oss \text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD}=250V, I_D=6A,$ $R_G=4.7\Omega, V_{GS}=10V$	30 15 40 10	ns ns ns ns	ns ns ns ns	ns ns ns ns
t_r	Rise time					
$t_{d(off)}$	Turn-off delay time					
t_f	Fall time					

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD} $I_{SDM}^{(1)}$	Source-drain current			12 48	A A	A
	Source-drain current (pulsed)					
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=12A, V_{GS}=0$			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=12A, V_{DD}=100V$ $di/dt = 100A/\mu s, T_j=25^\circ C$		300 3 22		ns μC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=12A, V_{DD}=100V$ $di/dt=100A/\mu s, T_j=150^\circ C$		370 4 22		ns μC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for TO-220 / D²PAK / I²PAK

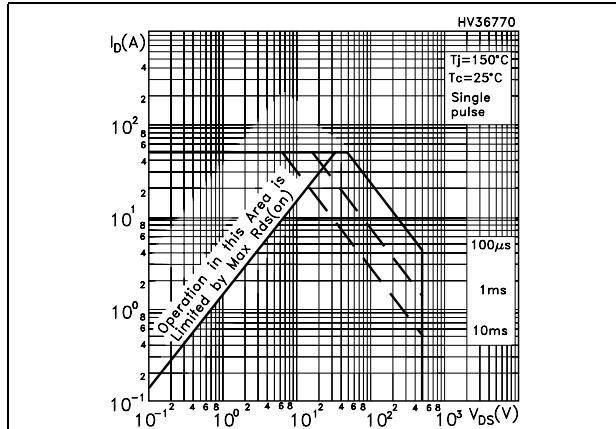


Figure 2. Thermal impedance for TO-220 / D²PAK / I²PAK

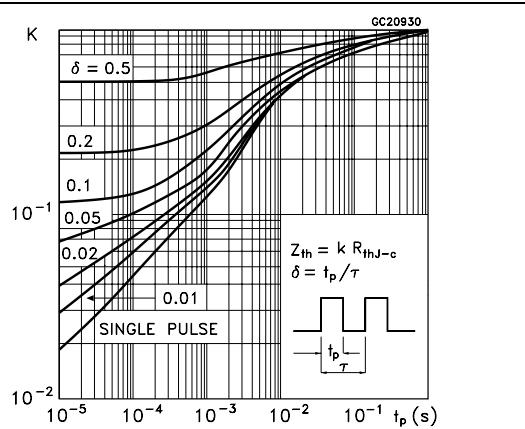


Figure 3. Safe operating area for TO-220FP

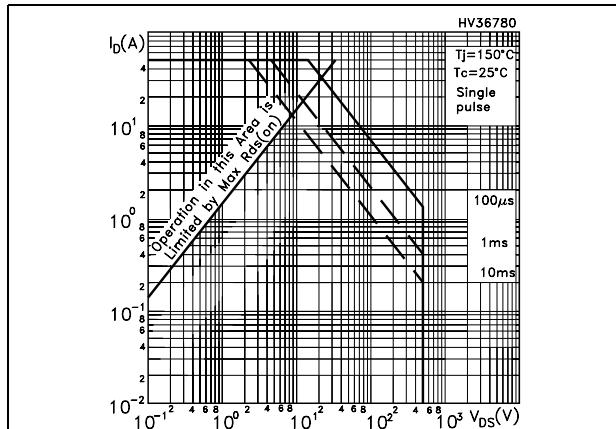


Figure 4. Thermal impedance for TO-220FP

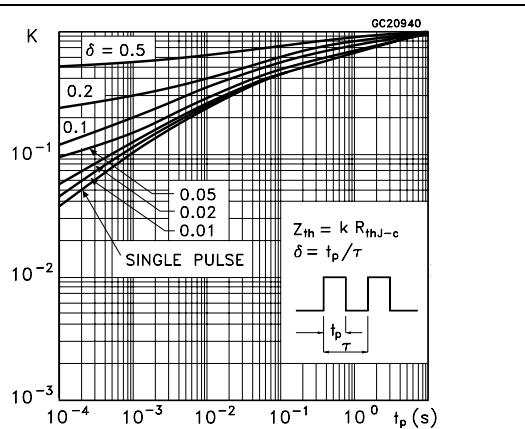


Figure 5. Safe operating area for TO-247

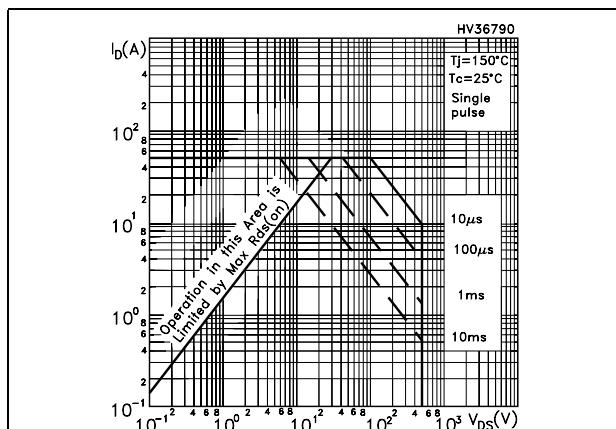


Figure 6. Thermal impedance for TO-247

