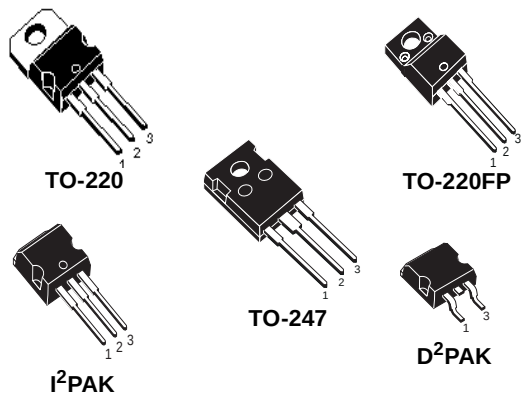
# STP13NK60Z/FP, STB13NK60Z STB13NK60Z-1, STW13NK60Z

N-CHANNEL 600V-0.48Ω-13A TO-220/FP/D$^2$PAK/I$^2$PAK/TO-247
Zener-Protected SuperMESH™Power MOSFET

| TYPE | $V_{DSS}$ | $R_{DS(on)}$ | $I_D$ | Pw |
|---|---|---|---|---|
| STP13NK60Z | 600 V | < 0.55 Ω | 13 A | 150 W |
| STP13NK60ZFP | 600 V | < 0.55 Ω | 13 A | 35 W |
| STB13NK60Z | 600 V | < 0.55 Ω | 13 A | 150 W |
| STB13NK60Z-1 | 600 V | < 0.55 Ω | 13 A | 150 W |
| STW13NK60Z | 600 V | < 0.55 Ω | 13 A | 150 W |

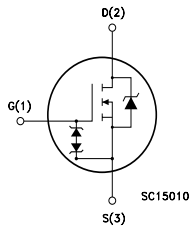
- TYPICAL $R_{DS}$(on) = 0.48 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- GATE CHARGE MINIMIZED
- VERY LOW INTRINSIC CAPACITANCES
- VERY GOOD MANUFACTURING REPEATIBILITY




## DESCRIPTION

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

**INTERNAL SCHEMATIC DIAGRAM**




## APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- IDEAL FOR OFF-LINE POWER SUPPLIES, ADAPTORS AND PFC
- LIGHTING

## ORDERING INFORMATION

| SALES TYPE | MARKING | PACKAGE | PACKAGING |
|---|---|---|---|
| STP13NK60Z | P13NK60Z | TO-220 | TUBE |
| STP13NK60ZFP | P13NK60ZFP | TO-220FP | TUBE |
| STB13NK60ZT4 | B13NK60Z | D$^2$PAK | TAPE & REEL |
| STB13NK60Z | B13NK60Z | D$^2$PAK | TUBE (ONLY UNDER REQUEST) |
| STB13NK60Z-1 | B13NK60Z | I$^2$PAK | TUBE |
| STW13NK60Z | W13NK60Z | TO-247 | TUBE |

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | | Unit |
|---|---|---|---|---|
| | | STP13NK60Z<br>STB13NK60Z/-1<br>STW13NK60Z | STP13NK60ZFP | |
| $V_{DS}$ | Drain-source Voltage ($V_{GS}$ = 0) | 600 | | V |
| $V_{DGR}$ | Drain-gate Voltage ($R_{GS}$ = 20 kΩ) | 600 | | V |
| $V_{GS}$ | Gate- source Voltage | ± 30 | | V |
| $I_D$ | Drain Current (continuous) at $T_C$ = 25°C | 13 | 13 (*) | A |
| $I_D$ | Drain Current (continuous) at $T_C$ = 100°C | 8.2 | 8.2 (*) | A |
| $I_{DM}$ (•) | Drain Current (pulsed) | 52 | 52 (*) | A |
| $P_{TOT}$ | Total Dissipation at $T_C$ = 25°C | 150 | 35 | W |
| | Derating Factor | 1.20 | 0.27 | W/°C |
| $V_{ESD(G-S)}$ | Gate source ESD(HBM-C=100pF, R=1.5KΩ) | 4000 | | V |
| dv/dt (1) | Peak Diode Recovery voltage slope | 4.5 | | V/ns |
| $V_{ISO}$ | Insulation Withstand Voltage (DC) | - | 2500 | V |
| $T_j$<br>$T_{stg}$ | Operating Junction Temperature<br>Storage Temperature | -55 to 150 | | °C |

(●) Pulse width limited by safe operating area
(1) $I_{SD}$ ≤13 A, di/dt ≤200A/µs, $V_{DD}$ ≤ $V_{(BR)DSS}$, $T_j$ ≤ $T_{JMAX}$.
(*) Limited only by maximum temperature allowed

## THERMAL DATA

| | | TO-220<br>$I^2PAK$<br>TO-247 | $D^2PAK$ | TO-220FP | |
|---|---|---|---|---|---|
| Rthj-case | Thermal Resistance Junction-case Max | 0.83 | | 3.6 | °C/W |
| Rthj-pcb | Thermal Resistance Junction-pcb Max (#) | | 60 | | °C/W |
| Rthj-amb | Thermal Resistance Junction-ambient Max | 62.5 | | | °C/W |
| $T_l$ | Maximum Lead Temperature For Soldering Purpose | 300 | | | °C |

## AVALANCHE CHARACTERISTICS

| Symbol | Parameter | Max Value | Unit |
|---|---|---|---|
| $I_{AR}$ | Avalanche Current, Repetitive or Not-Repetitive<br>(pulse width limited by $T_j$ max) | 10 | A |
| $E_{AS}$ | Single Pulse Avalanche Energy<br>(starting $T_j$ = 25 °C, $I_D$ = $I_{AR}$, $V_{DD}$ = 50 V) | 400 | mJ |

## GATE-SOURCE ZENER DIODE

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $BV_{GSO}$ | Gate-Source Breakdown Voltage | Igs=± 1mA (Open Drain) | 30 | | | V |

(#) When mounted on minimum Footprint

## PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

**ELECTRICAL CHARACTERISTICS** ($T_{CASE}$ =25°C UNLESS OTHERWISE SPECIFIED)

ON/OFF

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source Breakdown Voltage | $I_D$ = 1 mA, $V_{GS}$ = 0 | 600 | | | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current ($V_{GS}$ = 0) | $V_{DS}$ = Max Rating<br>$V_{DS}$ = Max Rating, $T_C$ = 125 °C | | | 1<br>50 | µA<br>µA |
| $I_{GSS}$ | Gate-body Leakage Current ($V_{DS}$ = 0) | $V_{GS}$ = ± 20 V | | | ±10 | µA |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 100 µA | 3 | 3.75 | 4.5 | V |
| $R_{DS(on)}$ | Static Drain-source On Resistance | $V_{GS}$ = 10 V, $I_D$ = 5 A | | 0.48 | 0.55 | Ω |

DYNAMIC

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $g_{fs}$ (1) | Forward Transconductance | $V_{DS}$ = 8 V, $I_D$ = 5 A | | 11 | | S |
| $C_{iss}$<br>$C_{oss}$<br>$C_{rss}$ | Input Capacitance<br>Output Capacitance<br>Reverse Transfer Capacitance | $V_{DS}$ = 25 V, f = 1 MHz, $V_{GS}$ = 0 | | 2030<br>210<br>48 | | pF<br>pF<br>pF |
| $C_{oss\ eq.}$ (3) | Equivalent Output Capacitance | $V_{GS}$ = 0V, $V_{DS}$ = 0V to 480 V | | 125 | | pF |

SWITCHING ON

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$<br>$t_r$ | Turn-on Delay Time<br>Rise Time | $V_{DD}$ = 300 V, $I_D$ = 5 A<br>$R_G$ = 4.7Ω $V_{GS}$ = 10 V<br>(Resistive Load see, Figure 3) | | 22<br>14 | | ns<br>ns |
| $Q_g$<br>$Q_{gs}$<br>$Q_{gd}$ | Total Gate Charge<br>Gate-Source Charge<br>Gate-Drain Charge | $V_{DD}$ = 480 V, $I_D$ = 10 A,<br>$V_{GS}$ = 10 V | | 66<br>11<br>33 | 92 | nC<br>nC<br>nC |

SWITCHING OFF

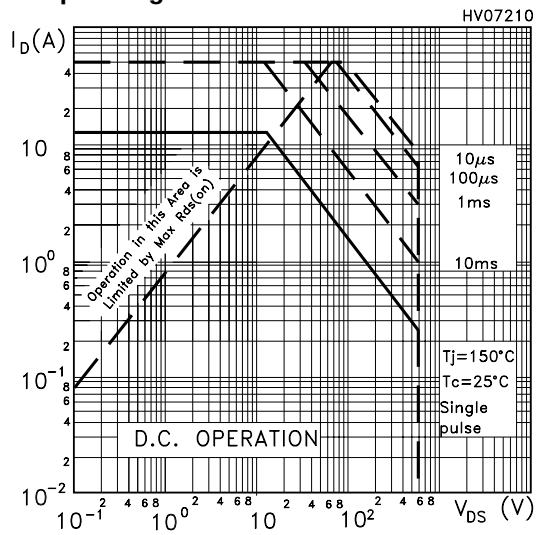
| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(off)}$<br>$t_f$ | Turn-off Delay Time<br>Fall Time | $V_{DD}$ = 300 V, $I_D$ = 5 A<br>$R_G$ = 4.7Ω $V_{GS}$ = 10 V<br>(Resistive Load see, Figure 3) | | 61<br>12 | | ns<br>ns |
| $t_{r(Voff)}$<br>$t_f$<br>$t_c$ | Off-voltage Rise Time<br>Fall Time<br>Cross-over Time | $V_{DD}$ = 480V, $I_D$ = 10 A,<br>$R_G$ = 4.7Ω, $V_{GS}$ = 10V<br>(Inductive Load see, Figure 5) | | 10<br>9<br>20 | | ns<br>ns<br>ns |

SOURCE DRAIN DIODE

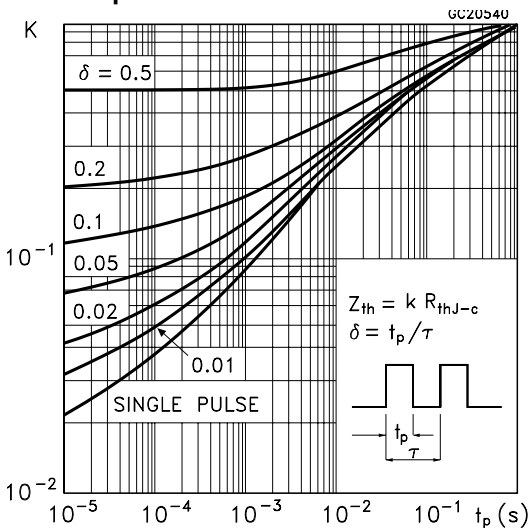
| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$<br>$I_{SDM}$ (2) | Source-drain Current<br>Source-drain Current (pulsed) | | | | 10<br>40 | A<br>A |
| $V_{SD}$ (1) | Forward On Voltage | $I_{SD}$ = 10 A, $V_{GS}$ = 0 | | | 1.6 | V |
| $t_{rr}$<br>$Q_{rr}$<br>$I_{RRM}$ | Reverse Recovery Time<br>Reverse Recovery Charge<br>Reverse Recovery Current | $I_{SD}$ = 10 A, di/dt = 100 A/µs<br>$V_{DD}$ = 35 V, $T_j$ = 150°C<br>(see test circuit, Figure 5) | | 570<br>4.5<br>16 | | ns<br>µC<br>A |

Note: 1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
2. Pulse width limited by safe operating area.
3. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as $C_{oss}$ when $V_{DS}$ increases from 0 to 80% $V_{DSS}$.

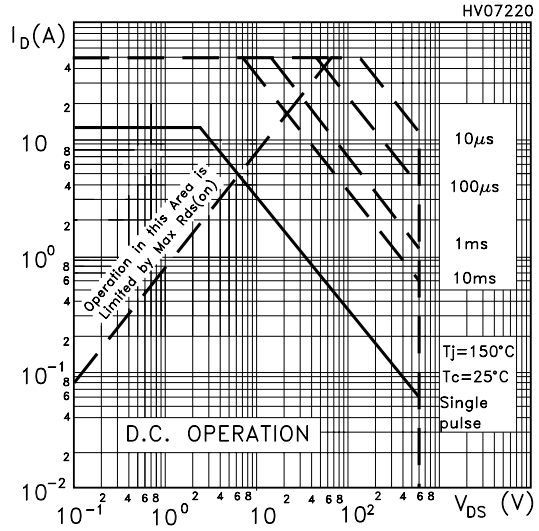
### Safe Operating Area For TO-220/D²PAK/I²PAK



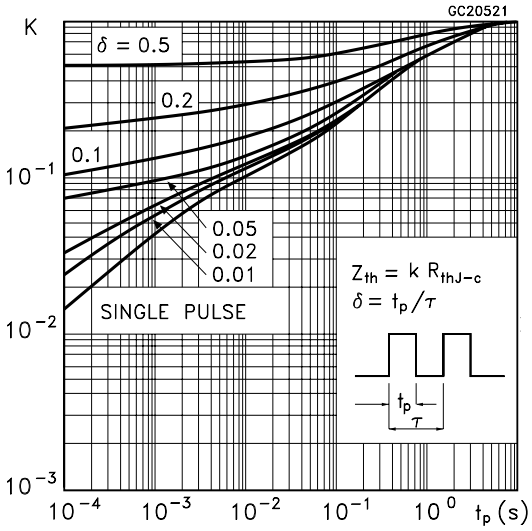

### Thermal Impedance For TO-220/D²PAK/I²PAK



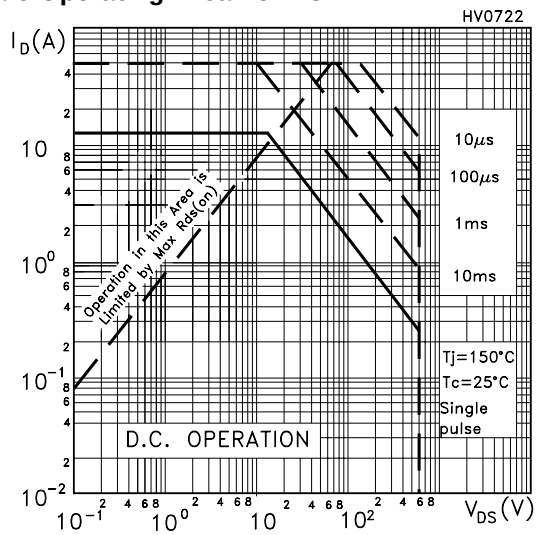

### Safe Operating Area For TO-220FP




### Thermal Impedance For TO-220FP




### Safe Operating Area For TO-247




### Thermal Impedance For TO-247