# STB13N80K5, STF13N80K5, STP13N80K5

## N-channel 800 V, 0.37 Ω, 12 A Zener-protected SuperMESH™ 5 Power MOSFET in D²PAK, TO-220FP and TO-220 packages

**Datasheet - production data**

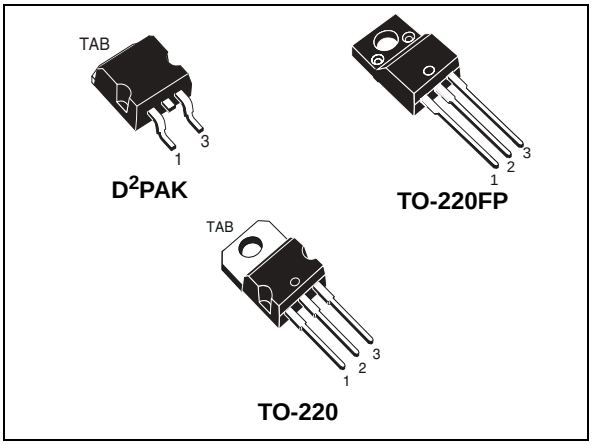
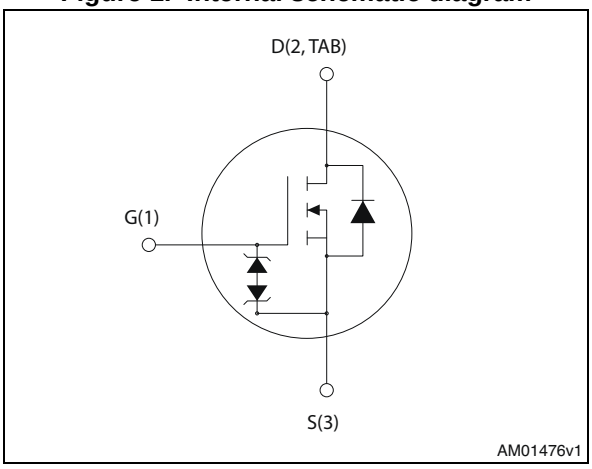



**Figure 1. Internal schematic diagram**




## Features

| Order codes | $V_{DSS}$ | $R_{DS(on)}$ | $I_D$ | $P_{TOT}$ |
|---|---|---|---|---|
| STB13N80K5 | 800 V | < 0.45 Ω | 12 A | 190 W |
| STF13N80K5 | 800 V | < 0.45 Ω | 12 A | 35 W |
| STP13N80K5 | 800 V | < 0.45 Ω | 12 A | 190 W |

- Worldwide best FOM (figure of merit)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected

## Applications

- Switching applications

## Description

These devices are N-channel Zener-protected Power MOSFETs realized in SuperMESH™ 5, a revolutionary avalanche-rugged very high voltage Power MOSFET technology based on an innovative proprietary vertical structure. The result is a drastic reduction in on-resistance and ultra low gate charge for applications which require superior power density and high efficiency.

**Table 1. Device summary**

| Order codes | Marking | Packages | Packaging |
|---|---|---|---|
| STB13N80K5 | 13N80K5 | D²PAK | Tape and reel |
| STF13N80K5 | 13N80K5 | TO-220FP | Tube |
| STP13N80K5 | 13N80K5 | TO-220 | Tube |

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

| Symbol | Parameter | Value | | Unit |
|---|---|---|---|---|
| | | D²PAK, TO-220 | TO-220FP | |
| $V_{GS}$ | Gate-source voltage | ± 30 | | V |
| $I_D$ | Drain current (continuous) at $T_C$ = 25 °C | 12 | 12(1) | A |
| $I_D$ | Drain current (continuous) at $T_C$ = 100 °C | 7.6 | 7.6 (1) | A |
| $I_{DM}$ (2) | Drain current (pulsed) | 48 | 48 (1) | A |
| $P_{TOT}$ | Total dissipation at $T_C$ = 25 °C | 190 | 35 | W |
| $I_{AR}$ | Max current during repetitive or single pulse avalanche (pulse width limited by $T_{jmax}$ ) | 4 | | A |
| $E_{AS}$ | Single pulse avalanche energy (starting $T_J$ = 25 °C, $I_D$=$I_{AS}$, $V_{DD}$= 50 V) | 148 | | mJ |
| $V_{iso}$ | Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s;$T_C$=25 °C) | | 2500 | V |
| dv/dt (3) | Peak diode recovery voltage slope | 4.5 | | V/ns |
| dv/dt(4) | MOSFET dv/dt ruggedness | 50 | | V/ns |
| $T_j$<br>$T_{stg}$ | Operating junction temperature<br>Storage temperature | -55 to 150 | | °C |

1. Limited by package.
2. Pulse width limited by safe operating area.
3. $I_{SD} \leq$ 12 A, di/dt $\leq$ 100 A/µs, $V_{Peak} \leq V_{(BR)DSS}$
4. $V_{DS} \leq$ 640 V

**Table 3. Thermal data**

| Symbol | Parameter | Value | | | Unit |
|---|---|---|---|---|---|
| | | D²PAK | TO-220 | TO-220FP | |
| Rthj-case | Thermal resistance junction-case max | 0.66 | | 3.57 | °C/W |
| Rthj-amb | Thermal resistance junction-amb max | | 62.5 | | |
| Rthj-pcb(1) | Thermal resistance junction-pcb max | 30 | | | |

1. When mounted on 1inch² FR-4 board, 2 oz Cu.

# 2 Electrical characteristics

($T_{CASE}$ = 25 °C unless otherwise specified).

**Table 4. On/off states**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage ($V_{GS}$= 0) | $I_D$ = 1 mA | 800 | | | V |
| $I_{DSS}$ | Zero gate voltage drain current ($V_{GS}$ = 0) | $V_{DS}$ = 800 V<br>$V_{DS}$ = 800 V, Tc=125 °C | | | 1<br>50 | µA<br>µA |
| $I_{GSS}$ | Gate body leakage current ($V_{DS}$ = 0) | $V_{GS}$ = ± 20 V | | | ±10 | µA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 100 µA | 3 | 4 | 5 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS}$ = 10 V, $I_D$= 6 A | | 0.37 | 0.45 | Ω |

**Table 5. Dynamic**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $C_{iss}$ | Input capacitance | $V_{DS}$ =100 V, f=1 MHz, $V_{GS}$=0 | - | 870 | - | pF |
| $C_{oss}$ | Output capacitance | | - | 50 | - | pF |
| $C_{rss}$ | Reverse transfer capacitance | | - | 2 | - | pF |
| $C_{o(tr)}$(1) | Equivalent capacitance time related | $V_{GS}$ = 0, $V_{DS}$ = 0 to 640 V | - | 110 | - | pF |
| $C_{o(er)}$(2) | Equivalent capacitance energy related | | - | 43 | - | pF |
| $R_G$ | Intrinsic gate resistance | f = 1MHz, $I_D$=0 | - | 5 | - | Ω |
| $Q_g$ | Total gate charge | $V_{DD}$ = 640 V, $I_D$ = 12 A<br>$V_{GS}$ =10 V | - | 29 | - | nC |
| $Q_{gs}$ | Gate-source charge | | - | 7 | | nC |
| $Q_{gd}$ | Gate-drain charge | | - | 18 | | nC |

1. Time related is defined as a constant equivalent capacitance giving the same charging time as $C_{oss}$ when $V_{DS}$ increases from 0 to 80% $V_{DSS}$
2. Energy related is defined as a constant equivalent capacitance giving the same stored energy as $C_{oss}$ when $V_{DS}$ increases from 0 to 80% $V_{DSS}$

**Table 6. Switching times**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD}$ = 400 V, $I_D$ = 6A, $R_G$=4.7 Ω, $V_{GS}$=10 V | - | 16 | - | ns |
| $t_r$ | Rise time | | - | 16 | - | ns |
| $t_{d(off)}$ | Turn-off delay time | | - | 42 | - | ns |
| $t_f$ | Fall time | | - | 16 | - | ns |

**Table 7. Source drain diode**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$ | Source-drain current | | - | | 14 | A |
| $I_{SDM}$ | Source-drain current (pulsed) | | - | | 56 | A |
| $V_{SD}$(1) | Forward on voltage | $I_{SD}$= 12 A, $V_{GS}$=0 | - | | 1.5 | V |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$= 12 A, $V_{DD}$= 60 V di/dt = 100 A/µs, | - | 406 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 5.7 | | µC |
| $I_{RRM}$ | Reverse recovery current | | - | 28 | | A |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$= 12 A,$V_{DD}$= 60 V di/dt=100 A/µs, Tj=150 °C | - | 600 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 7.9 | | µC |
| $I_{RRM}$ | Reverse recovery current | | - | 26 | | A |

1. Pulsed: pulse duration = 300µs, duty cycle 1.5%

**Table 8. Gate-source Zener diode**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)GSO}$ | Gate-source breakdown voltage | $I_{GS}$= ± 1mA, $I_D$= 0 | 30 | - | - | V |

The built-in back-to-back Zener diodes have been specifically designed to enhance not only the device's ESD capability, but also to make them capable of safely absorbing any voltage transients that may occasionally be applied from gate to source. In this respect, the Zener voltage is appropriate to achieve efficient and cost-effective protection of device integrity. The integrated Zener diodes thus eliminate the need for external components.

## 2.1 Electrical characteristics (curves)

**Figure 2. Safe operating area for D$^2$PAK**

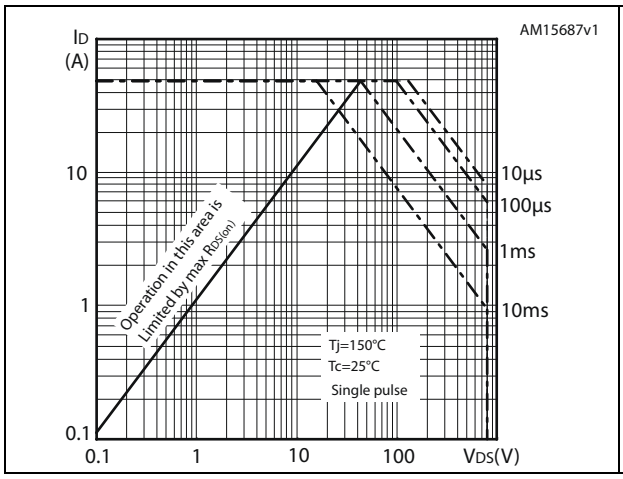



**Figure 3. Thermal impedance for D$^2$PAK**

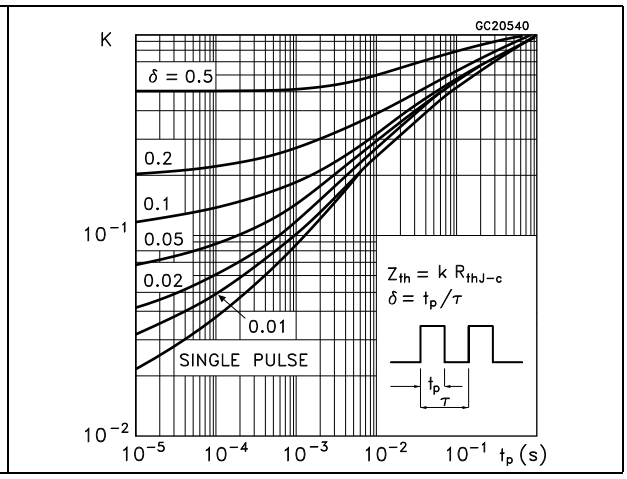



**Figure 4. Safe operating area for TO-220FP**

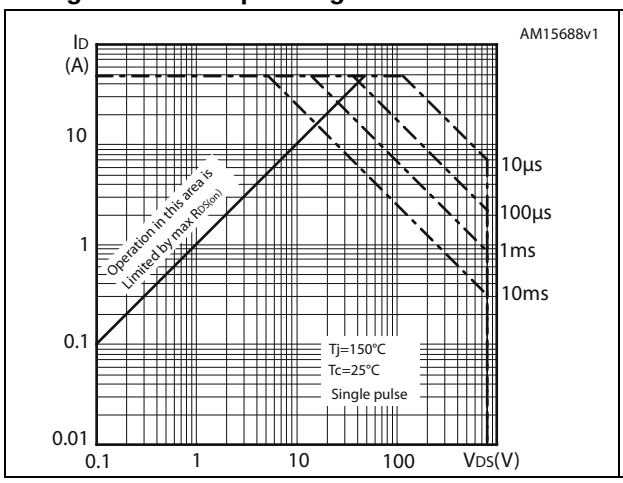



**Figure 5. Thermal impedance for TO-220FP**

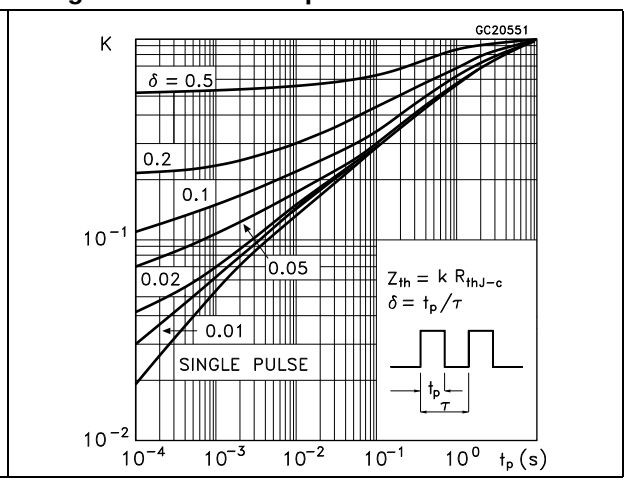



**Figure 6. Safe operating area for TO-220**

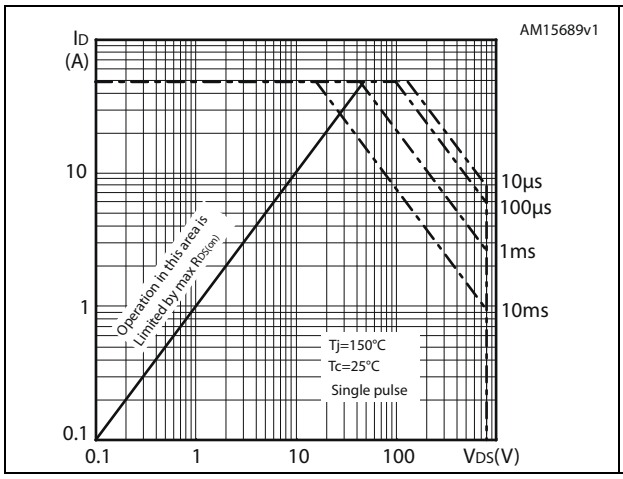



**Figure 7. Thermal impedance for TO-220**