STB12NK80Z
STP12NK80Z - STW12NK80Z

N-CHANNEL 800V - 0.65Ω - 10.5A - TO220-D²PAK-TO247
Zener-Protected SuperMESH™ MOSFET

General features

Type	V_{DSS}	$R_{DS(on)}$	I_D	Pw
STB12NK80Z	800 V	<0.75 Ω	10.5 A	190 W
STP12NK80Z	800 V	<0.75 Ω	10.5 A	190 W
STW12NK80Z	800 V	<0.75 Ω	10.5 A	190 W

- EXTREMELY HIGH dv/dt CAPABILITY
- IMPROVED ESD CAPABILITY
- 100% AVALANCHE TESTED
- GATE CHARGE MINIMIZED
- VERY LOW INTRINSIC CAPACITANCES
- VERY GOOD MANUFACTURING REPEABILITY

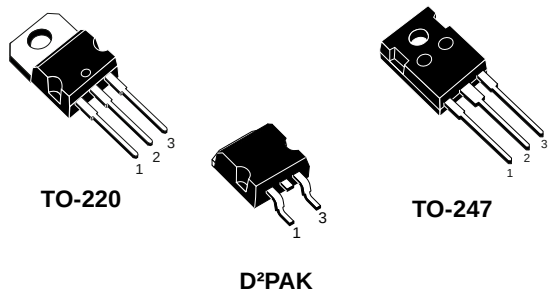
Description

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications.

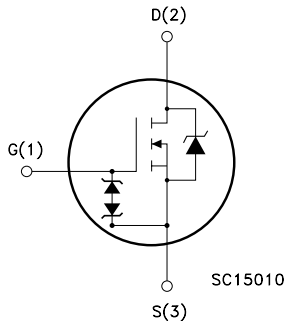
Applications

- HIGH CURRENT, HIGH SPEED SWITCHING
- IDEAL FOR OFF-LINE POWER SUPPLIES, ADAPTOR AND PFC

Package



Internal schematic diagram



Order codes

Sales Type	Marking	Package	Packaging
STB12NK80ZT4	B12NK80Z	D²PAK	TAPE & REEL
STP12NK80Z	P12NK80Z	TO-220	TUBE
STW12NK80Z	W12NK80Z	TO-247	TUBE

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-Source Voltage (V_{GS} = 0)	800	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20kΩ)	800	V
V_{GS}	Gate-Source Voltage	± 30	V
I_D	Drain Current (continuous) at T_C = 25°C	10.5	A
I_D	Drain Current (continuous) at T_C = 100°C	6.6	A
I_{DM} *Note* 2	Drain Current (pulsed)	42	A
P_{TOT}	Total Dissipation at T_C = 25°C	190	W
	Derating Factor	1.51	W/°C
Vesd(G-S)	G-S ESD (HBM C=100pF, R=1.5kΩ)	6000	V
dv/dt *Note* 1	Peak Diode Recovery voltage slope	4.5	V/ns
T_j T_{stg}	Operating Junction Temperature Storage Temperature	-55 to 150	°C

Table 2. Thermal data

		TO-220/D²PAK	TO-247	Unit
Rthj-case	Thermal Resistance Junction-case Max	0.66		°C/W
Rthj-amb	Thermal Resistance Junction-amb Max	62.5	50	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose	300		°C

Table 3. Avalanche characteristics

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, repetitive or Not-Repetitive (pulse width limited by Tj max)	10.5	A
E_{AS}	Single Pulse Avalanche Energy (starting Tj=25°C, I_D=I_{AR}, V_{DD}= 50V)	400	mJ

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	I_D = 1mA, V_{GS}= 0	800			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating, V_{DS} = Max Rating,Tc = 125°C			1 50	µA µA
I_{GSS}	Gate Body Leakage Current (V_{DS} = 0)	V_{GS} = ±20V			±10	µA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}= V_{GS}, I_D = 100 µA	3	3.75	4.5	V
$R_{DS(on)}$	Static Drain-Source On Resistance	V_{GS}= 10 V, I_D= 4.5 A		0.65	0.75	Ω

Table 5. Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} *Note* 4	Forward Transconductance	V_{DS} =15V, I_D = 5.25A		12		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} =25V, f=1 MHz, V_{GS}=0		2620 250 53		pF pF pF
$C_{oss\ eq.}$ *Note* 5	Equivalent Ouput Capacitance	V_{GS}=0, V_{DS} =0V to 640V		100		pF
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD}=640V, I_D = 10.5 A V_{GS} =10V (see Figure 17)		87 14 44		nC nC nC

Table 6. Switching times

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	V_{DD}=400 V, I_D=5.25 A, R_G=4.7Ω, V_{GS}=10V (see Figure 18)		30 18		ns ns
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	V_{DD}=400 V, I_D=5.25A, R_G=4.7Ω, V_{GS}=10V (see Figure 18)		70 20		ns ns
$t_{r(Voff)}$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	V_{DD}=640 V, I_D=10.5A, R_G=4.7Ω, V_{GS}=10V (see Figure 18)		16 15 28		ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} *Note* 2	Source-drain Current Source-drain Current (pulsed)				10.5 42	A A
V_{SD} *Note* 4	Forward on Voltage	I_{SD}=10.5 A, V_{GS}=0			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD}=10.5A, di/dt = 100A/µs, V_{DD}=100 V, Tj=150°C		635 5.9 18.5		ns µC A

Table 8. Gate-source zener diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{GSO} *Note* 6	Gate-Source Breakdown Voltage	Igs=±1mA (Open Drain)	30			V

(1) I_{SD} ≤10.5 A, di/dt ≤200A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$

(2) Pulse width limited by safe operating area

(3) Limited only by maximum temperature allowed

(4) Pulsed: pulse duration = 300µs, duty cycle 1.5%

(5) $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80%V_{DSS}

(6)The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.