STD10P6F6, STP10P6F6

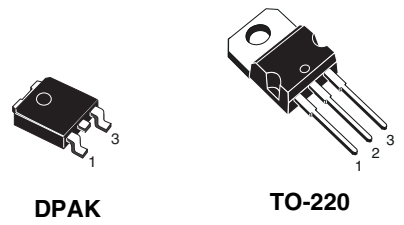
P-channel 60 V, 0.15 Ω typ., 10 A STripFET™ VI DeepGATE™ Power MOSFET in DPAK and TO-220 packages

Datasheet — preliminary data

Features

Order codes	V_{DSS}	$R_{DS(on)}$ max	I_D
STD10P6F6	60 V	0.18 Ω	10 A
STP10P6F6	60 V	0.18 Ω	10 A

- $R_{DS(on)}$ * Q_g industry benchmark
- Extremely low on-resistance $R_{DS(on)}$
- High avalanche ruggedness
- Low gate drive power losses



Applications

- Switching applications

Description

These devices are P-channel Power MOSFETs developed using the 6th generation of STripFET™ DeepGATE™ technology, with a new gate structure. The resulting Power MOSFETs exhibits the lowest $R_{DS(on)}$ in all packages.

Figure 1. Internal schematic diagram

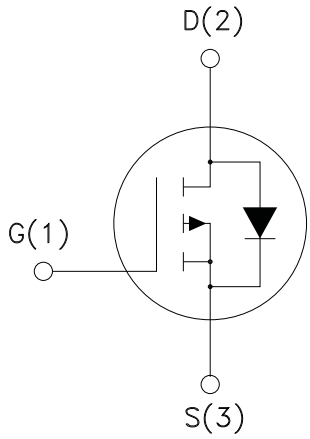


Table 1. Device summary

Order codes	Marking	Package	Packaging
STD10P6F6	10P6F6	DPAK	Tape and reel
STP10P6F6	10P6F6	TO-220	Tube

Note: For the P-channel Power MOSFET the actual polarity of the voltages and the current must be reversed.

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	60	V
V_{GS}	Gate-source voltage	± 20	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	10	A
I_D	Drain current (continuous) at T_C = 100 °C	7.2	A
I_{DM} (2)	Drain current (pulsed)	40	A
P_{TOT}	Total dissipation at T_C = 25 °C	35	W
	Derating factor	0.23	W/°C
T_{stg}	Storage temperature	-55 to 175	°C
T_j	Max. operating junction temperature	175	°C

1. Limited by wire bonding
2. Pulse width limited by safe operating area

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		DPAK	TO-220	
$R_{thj-case}$	Thermal resistance junction-case max	4.29		°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient max	100	62.5	°C/W
T_l	Maximum lead temperature for soldering purpose	275	300	°C

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown Voltage	I_D = 250 µA, V_{GS}= 0	60			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 60 V V_{DS} = 60 V, Tc = 125 °C			1 10	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 5 A		0.15	0.18	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 48 V, f=1 MHz, V_{GS} = 0	-	360 55 28	-	pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 48V, I_D = 10 A V_{GS} = 10 V	-	7 1.4 2	-	nC nC nC

Table 6. Switching on/off (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	V_{DD} = 48 V, I_D = 5 A, R_G = 4.7 Ω, V_{GS} = 10 V	-	7.5 7	-	ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time		-	16.5 10	-	ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}(1)	Source-drain current Source-drain current (pulsed)		-		10 40	A A
V_{SD}(2)	Forward on voltage	I_{SD} = 5 A, V_{GS} = 0	-		1.1	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 10 A, di/dt = 100 A/µs, V_{DD} = 48 V	-	28 28 2		ns nC A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%