

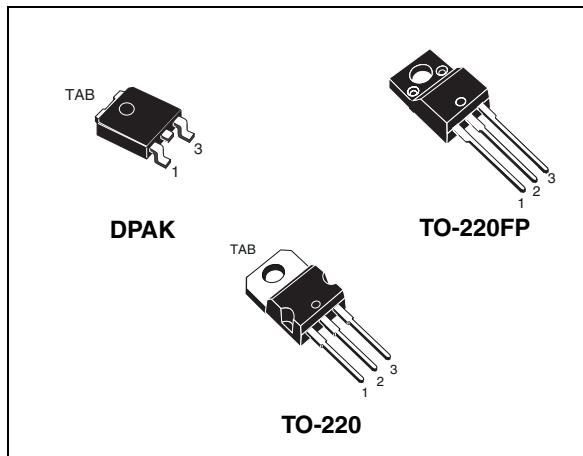
STD10NM60ND, STF10NM60ND STP10NM60ND

N-channel 600 V, 0.57 Ω, 8 A, DPAK, TO-220FP, TO-220
FDmesh™ II Power MOSFET (with fast diode)

Features

Order codes	V_{DSS} @ T_{Jmax}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STD10NM60ND				70 W
STF10NM60ND	650 V	< 0.6 Ω	8 A	25 W
STP10NM60ND				70 W

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance
- Extremely high dv/dt avalanche capabilities



Applications

- Switching applications

Description

This FDmesh™ II Power MOSFET with intrinsic fast-recovery body diode is produced using the second generation of MDmesh™ technology. Utilizing a new strip-layout vertical structure, this revolutionary device features extremely low on-resistance and superior switching performance. It is ideal for bridge topologies and ZVS phase-shift converters.

Figure 1. Internal schematic diagram

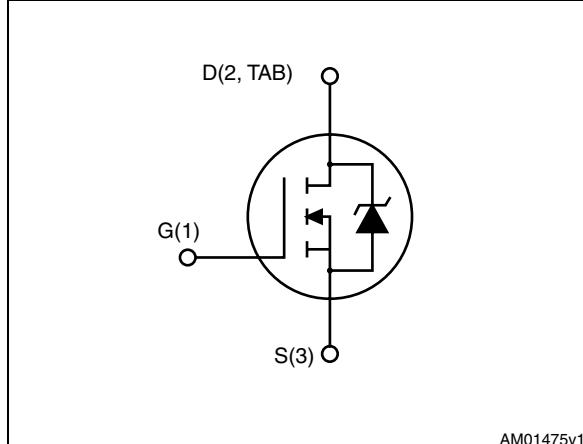


Table 1. Device summary

Order codes	Marking	Package	Packaging
STD10NM60ND	10NM60ND	DPAK	Tape and reel
STF10NM60ND		TO-220FP	
STP10NM60ND		TO-220	Tube

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value			Unit
		DPAK	TO-220FP	TO-220	
V_{DS}	Drain-source voltage		600		V
V_{GS}	Gate- source voltage		± 25		V
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$	8	8 ⁽¹⁾	8	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	5	5 ⁽¹⁾	5	A
$I_{DM}^{(2)}$	Drain current (pulsed)	32	32 ⁽¹⁾	32	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	70	25	70	W
$dv/dt^{(3)}$	Peak diode recovery voltage slope		40		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t=1\text{ s}; T_C=25^\circ\text{C}$)		2500		V
T_J T_{stg}	Operating junction temperature Storage temperature		- 55 to 150		$^\circ\text{C}$

1. Limited by maximum junction temperature.
2. Pulse width limited by safe operating area.
3. $I_{SD} \leq 8\text{ A}$, $dI/dt \leq 400\text{ A}/\mu\text{s}$, V_{DS} peak $\leq V_{(BR)DSS}$, $V_{DD} = 80\%$ $V_{(BR)DSS}$.

Table 3. Thermal data

Symbol	Parameter	Value			Unit
		DPAK	TO-220FP	TO-220	
$R_{thj-case}$	Thermal resistance junction-case max	1.79	5	1.79	$^\circ\text{C/W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.50		62.50	$^\circ\text{C/W}$
$R_{thj-pcb}$	Thermal resistance junction-pcb max	50			$^\circ\text{C/W}$
T_J	Maximum lead temperature for soldering purpose			300	$^\circ\text{C/W}$

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j Max)	2.5	A
E_{AS}	Single pulse avalanche energy (starting $T_J=25^\circ\text{C}$, $I_D=I_{AS}$, $V_{DD}=50\text{ V}$)	130	mJ

2 Electrical characteristics

(T_{case} =25 °C unless otherwise specified)

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage (V _{GS} = 0)	I _D = 1 mA	600			V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V _{DS} = 600 V V _{DS} = 600 V, T _C =125 °C			1 100	μA μA
I _{GSS}	Gate-body leakage current (V _{DS} = 0)	V _{GS} = ± 25 V			±100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	3	4	5	V
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 10 V, I _D = 4 A		0.57	0.6	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss} C _{oss} C _{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V _{DS} = 50 V, f = 1 MHz, V _{GS} = 0	-	577 32.4 1.76	-	pF pF pF
C _{oss eq} ⁽¹⁾	Equivalent capacitance time related	V _{DS} = 0 to 480 V, V _{GS} = 0	-	138	-	pF
R _g	Gate input resistance	f=1 MHz open drain	-	6	-	Ω
Q _g Q _{gs} Q _{gd}	Total gate charge Gate-source charge Gate-drain charge	V _{DD} = 480 V, I _D = 8 A, V _{GS} = 10 V	-	20 4.3 11.6	-	nC nC nC

1. C_{oss eq} time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
t _{d(on)} t _r t _{d(off)} t _f	Turn-on delay time Rise time Turn-off-delay time Fall time	V _{DD} = 300 V, I _D = 4 A, R _G = 4.7 Ω, V _{GS} = 10 V	-	9.2 10 32 9.8	-	ns ns ns ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD} $I_{SDM}^{(1)}$	Source-drain current		-		8	A
	Source-drain current (pulsed)				32	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 8 \text{ A}, V_{GS} = 0$	-		1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time	$I_{SD} = 8 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$	-	118		ns
	Reverse recovery charge			680		nC
	Reverse recovery current			11		A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time	$I_{SD} = 8 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$ $T_J = 150 \text{ }^\circ\text{C}$	-	150		ns
	Reverse recovery charge			918		nC
	Reverse recovery current			12		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for DPAK

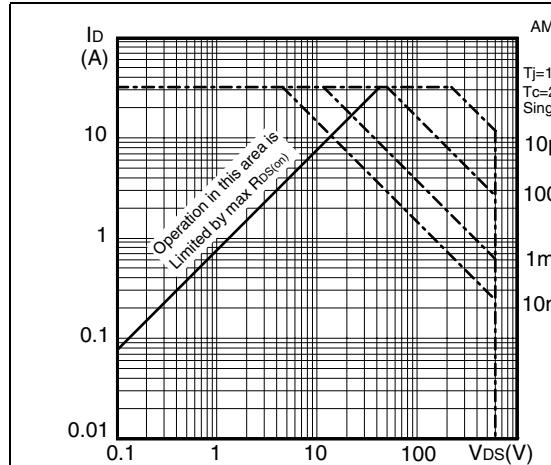


Figure 3. Thermal impedance for DPAK

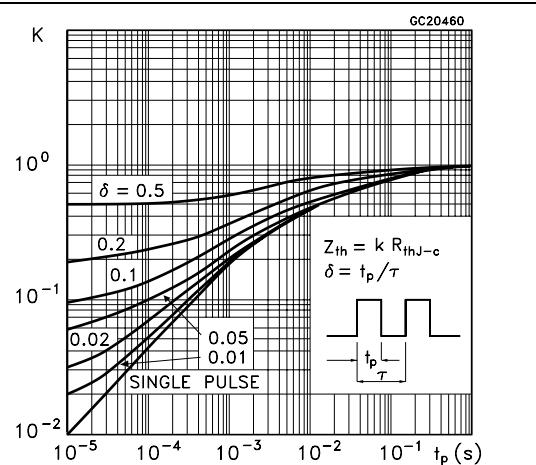


Figure 4. Safe operating area for TO-220FP

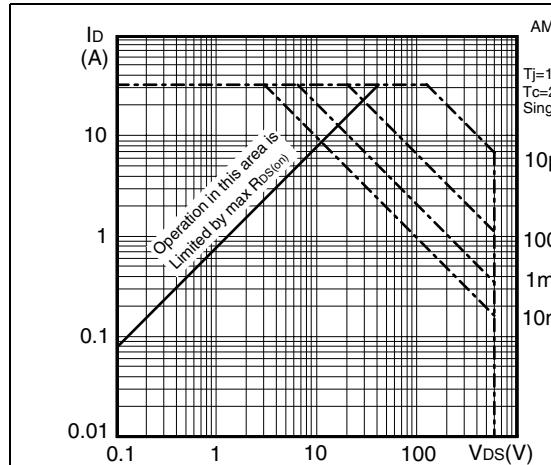


Figure 5. Thermal impedance for TO-220FP

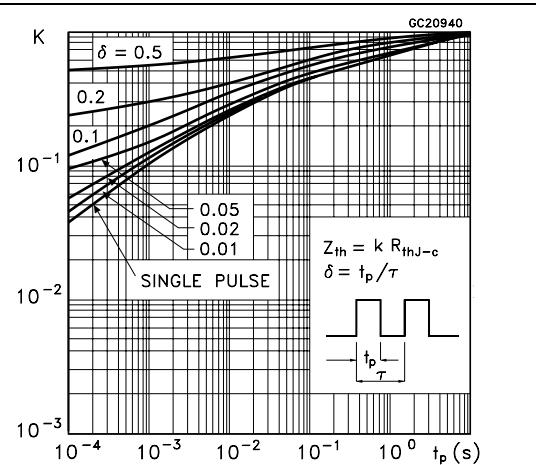


Figure 6. Safe operating area for TO-220

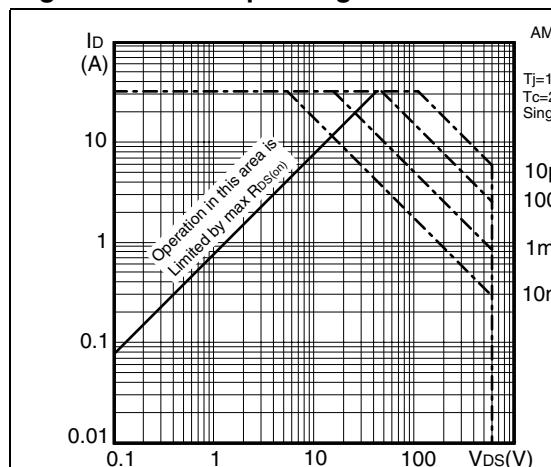


Figure 7. Thermal impedance for TO-220

