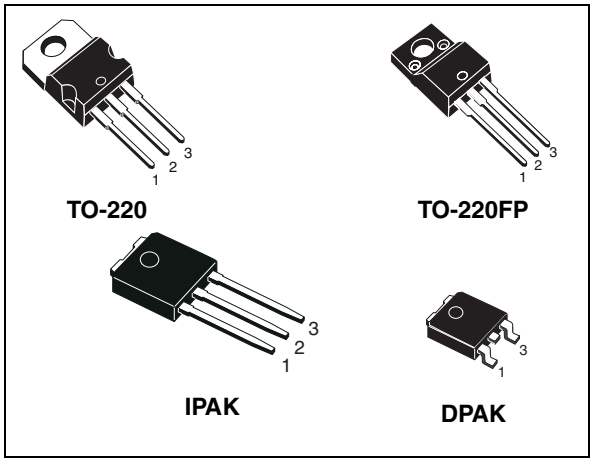
STD10NM60N, STF10NM60N STP10NM60N, STU10NM60N

N-channel 600 V, 0.53 Ω, 10 A, DPAK, TO-220, TO-220FP, IPAK
MDmesh™ II Power MOSFET

Features

Order codes	V_{DSS} @$T_J$max	$R_{DS(on)}$ max.	I_D	P_w
STD10NM60N	650 V	< 0.55 Ω	10 A	70 W
STF10NM60N				25 W
STP10NM60N				70 W
STU10NM60N				

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance



Application

Switching applications

Description

These devices are N-channel 600 V Power MOSFET realized using the second generation of MDmesh™ technology. It applies the benefits of the multiple drain process to STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product offers improved on-resistance, low gate charge, high dv/dt capability and excellent avalanche characteristics.

Figure 1. Internal schematic diagram

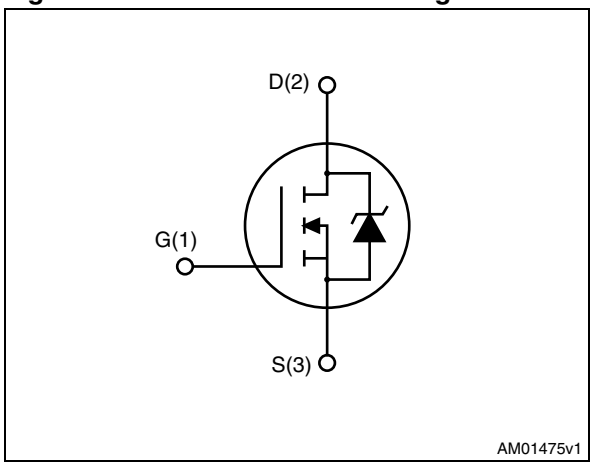


Table 1. Device summary

Order codes	Marking	Package	Packaging
STD10NM60N	10NM60N	DPAK	Tape and reel
STF10NM60N	10NM60N	TO-220FP	Tube
STP10NM60N	10NM60N	TO-220	Tube
STU10NM60N	10NM60N	IPAK	Tube

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value				Unit
		TO-220	TO-220FP	IPAK	DPAK	
V_{GS}	Gate- source voltage	± 25				V
I_D	Drain current (continuous) at T_C = 25 °C	10	10 (1)	10		A
I_D	Drain current (continuous) at T_C = 100 °C	5	5 (1)	5		A
I_{DM} (2)	Drain current (pulsed)	32	32 (1)	32		A
P_{TOT}	Total dissipation at T_C = 25 °C	70	25	70		W
dv/dt(3)	Peak diode recovery voltage slope	15				V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s;T_C=25 °C)		2500			V
T_J T_{stg}	Operating junction temperature Storage temperature	- 55 to 150				°C

1. Limited only by maximum temperature allowed.
2. Pulse width limited by safe operating area.
3. I_{SD} ≤10 A, di/dt ≤400 A/µs, V_{DS} peak ≤$V_{(BR)DSS}$, V_{DD} = 80% $V_{(BR)DSS}$.

Table 3. Thermal data

Symbol	Parameter	Value				Unit
		TO-220	TO-220FP	IPAK	DPAK	
$R_{thj-case}$	Thermal resistance junction-case max	1.79	5	1.79		°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.50		100		°C/W
$R_{thj-pcb}$	Thermal resistance junction-pcb max				50	°C/W
T_J	Maximum lead temperature for soldering purpose	300				°C/W

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by Tj Max)	4	A
E_{AS}	Single pulse avalanche energy (starting T_J=25 °C, I_D=I_{AS}, V_{DD}=50 V)	200	mJ

2 Electrical characteristics

(Tcase =25 °C unless otherwise specified)

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	600			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = max rating V_{DS} = max rating, T_C=125 °C			1 100	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 25 V; V_{DS}=0			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 4 A		0.53	0.55	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0	-	540 44 1.2	-	pF pF pF
$C_{oss\ eq}$(1)	Equivalent capacitance time related	V_{DS} = 0 to 480 V, V_{GS} = 0	-	110	-	pF
R_g	Gate input resistance	f=1 MHz open drain	-	6	-	Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 480 V, I_D = 8 A, V_{GS} = 10 V	-	19 3 10	-	nC nC nC

1. $C_{oss\ eq}$, time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 4 A, R_G = 4.7 Ω, V_{GS} = 10 V	-	10	-	ns
t_r	Rise time			12		ns
$t_{d(off)}$	Turn-off-delay time			32		ns
t_f	Fall time			15		ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current		-		8	A
I_{SDM} (1)	Source-drain current (pulsed)				32	A
V_{SD} (2)	Forward on voltage	I_{SD} = 8 A, V_{GS} = 0	-		1.3	V
t_{rr}	Reverse recovery time	I_{SD} = 8 A, di/dt = 100 A/µs V_{DD}= 60 V	-	250		ns
Q_{rr}	Reverse recovery charge			2.12		µC
I_{RRM}	Reverse recovery current			17		A
t_{rr}	Reverse recovery time	I_{SD} = 8 A, di/dt = 100 A/µs V_{DD}= 60 V T_J = 150 °C	-	315		ns
Q_{rr}	Reverse recovery charge			2.6		µC
I_{RRM}	Reverse recovery current			16.5		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220

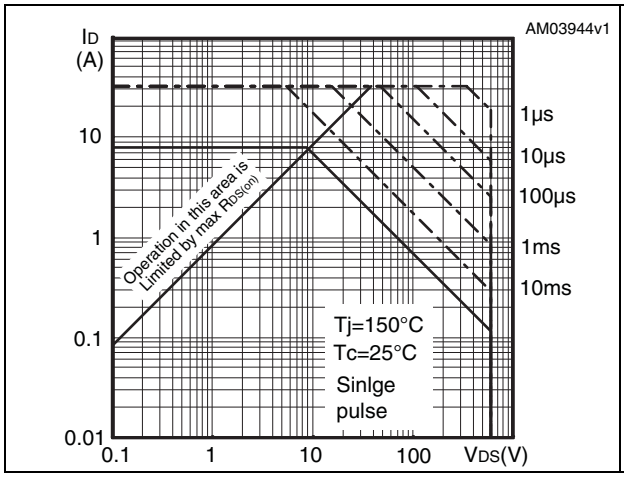


Figure 3. Thermal impedance for TO-220

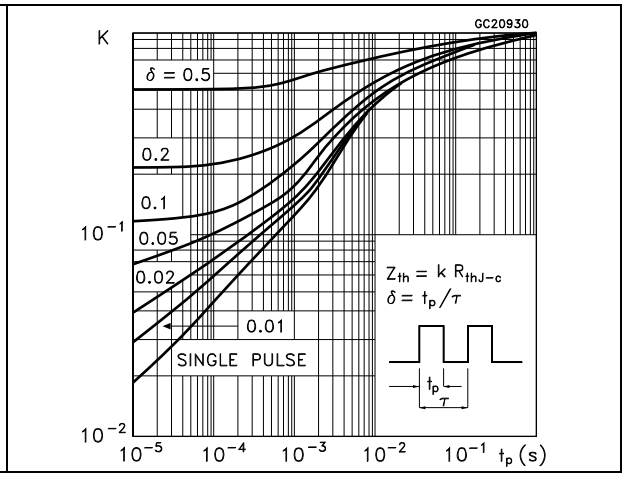


Figure 4. Safe operating area for TO-220FP

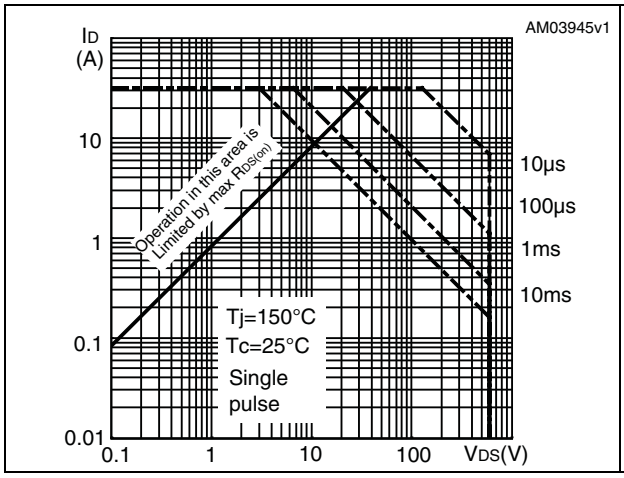


Figure 5. Thermal impedance for TO-220FP

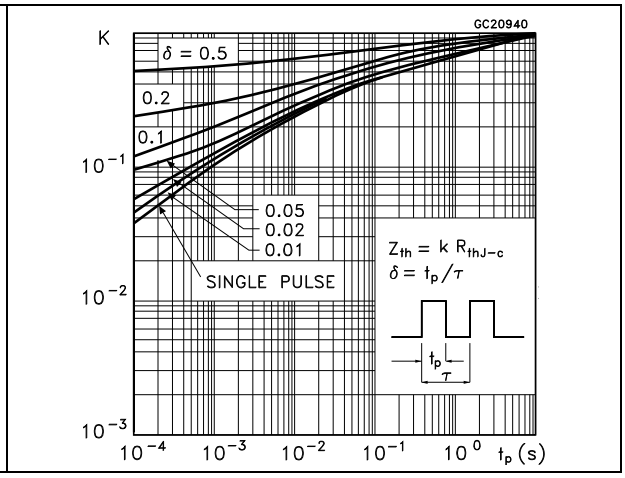


Figure 6. Safe operating area for DPAK, IPAK

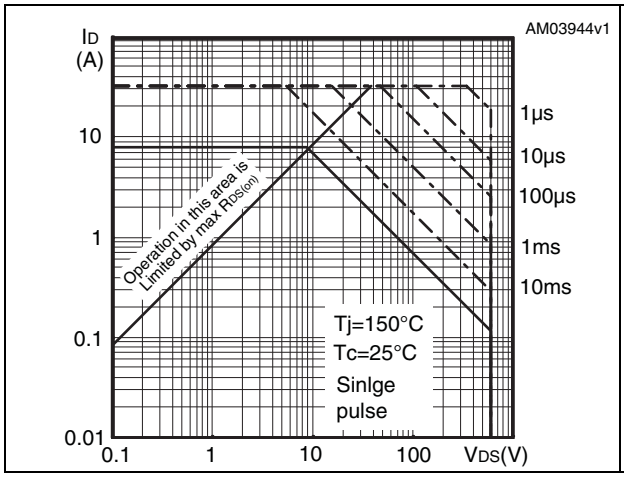


Figure 7. Thermal impedance for DPAK, IPAK