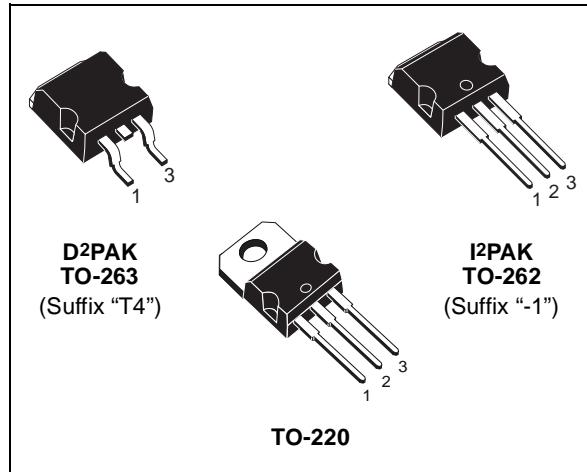


STB100NF03L-03 STP100NF03L-03 STB100NF03L-03-1

**N-CHANNEL 30V - 0.0026 Ω - 100A D²PAK/I²PAK/TO-220
STripFET™ II POWER MOSFET**

TYPE	V _{DSS}	R _{D(on)}	I _D
STB100NF03L-03	30 V	<0.0032 Ω	100 A
STP100NF03L-03	30 V	<0.0032 Ω	100 A
STB100NF03L-03-1	30 V	<0.0032 Ω	100 A

- TYPICAL R_{D(on)} = 0.0026 Ω
- LOW THRESHOLD DRIVE
- 100% AVALANCHE TESTED
- LOGIC LEVEL DEVICE
- THROUGH-HOLE IPA (TO-251) POWER PACKAGE IN TUBE (SUFFIX "-1")
- SURFACE-MOUNTING D²PAK (TO-263) POWER PACKAGE IN TUBE (NO SUFFIX) OR IN TAPE & REEL (SUFFIX "T4")



DESCRIPTION

This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

APPLICATIONS

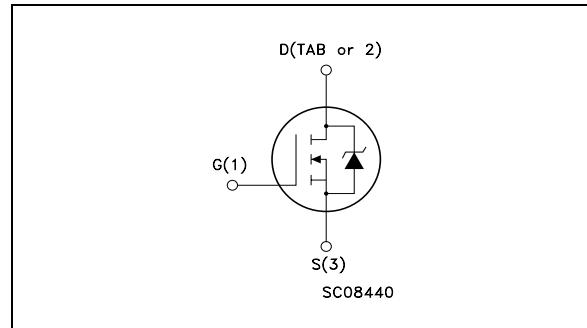
- HIGH CURRENT, HIGH SWITCHING SPEED
- MOTOR CONTROL, AUDIO AMPLIFIERS
- DC-DC & DC-AC CONVERTERS
- SOLENOID AND RELAY DRIVERS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	30	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	30	V
V _{GS}	Gate-source Voltage	± 16	V
I _{D(1)}	Drain Current (continuous) at T _C = 25°C	100	A
I _{D(1)}	Drain Current (continuous) at T _C = 100°C	100	A
I _{DM(•)}	Drain Current (pulsed)	400	A
P _{tot}	Total Dissipation at T _C = 25°C	300	W
	Derating Factor	2	W/°C
EAS(2)	Single Pulse Avalanche Energy	1.9	J
T _{stg}	Storage Temperature	-55 to 175	°C
T _j	Operating Junction Temperature		

(•) Pulse width limited by safe operating area
(1) Current Limited by Package

INTERNAL SCHEMATIC DIAGRAM



(2) Starting T_j = 25 °C, I_{AR} = 50A, V_{DD} = 50V

STB100NF03L-03 STP100NF03L-03 STB100NF03L-03-1

THERMAL DATA

R _{thj-case} R _{thj-amb} T _I	Thermal Resistance Junction-case Thermal Resistance Junction-ambient Maximum Lead Temperature For Soldering Purpose	Max Max	0.5 62.5 300	°C/W °C/W °C
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ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V(BR)DSS	Drain-source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0	30			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating T _C = 125°C			1 10	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 16V			±100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} I _D = 250 μA	1	1.7	2.5	V
R _{D(on)}	Static Drain-source On Resistance	V _{GS} = 10 V I _D = 50 A V _{GS} = 4.5 V I _D = 50 A		0.0026 0.0032	0.0032 0.0045	Ω Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (*)	Forward Transconductance	V _{DS} >I _{D(on)} ×R _{D(on)max} I _D =10 A	10			S
C _{iss} C _{oss} C _{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V _{DS} = 25V f = 1 MHz V _{GS} = 0		6200 1720 300		pF pF pF

STB100NF03L-03 STP100NF03L-03 STB100NF03L-03-1

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Time Rise Time	$V_{DD} = 15 \text{ V}$ $I_D = 50 \text{ A}$ $R_G = 4.7 \Omega$ $V_{GS} = 4.5 \text{ V}$ (Resistive Load, Figure 3)		35 315		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 24 \text{ V}$ $I_D = 100 \text{ A}$ $V_{GS} = 5 \text{ V}$		88 22.5 36		nC nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	$V_{DD} = 20 \text{ V}$ $I_D = 50 \text{ A}$ $R_G = 4.7 \Omega$, $V_{GS} = 4.5 \text{ V}$ (Resistive Load, Figure 3)		115 95		ns ns
$t_{r(Voff)}$ t_f t_c	Off-Voltage Rise Time Fall Time Cross-over Time	$V_{clamp} = 24 \text{ V}$ $I_D = 100 \text{ A}$ $R_G = 4.7 \Omega$ $V_{GS} = 4.5 \text{ V}$ (Inductive Load, Figure 5)		110 55 100		ns ns ns

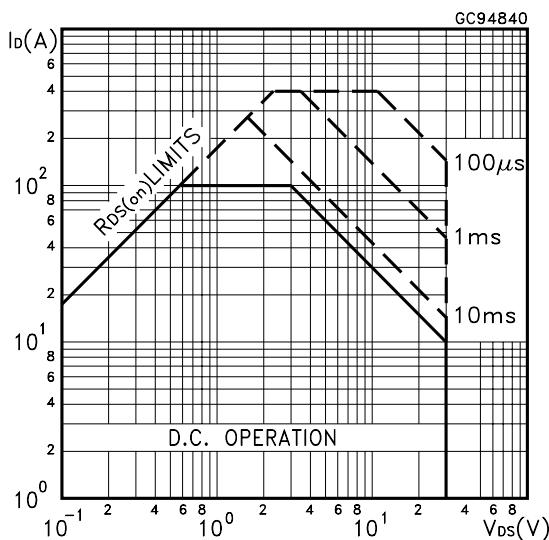
SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM} (\bullet)$	Source-drain Current Source-drain Current (pulsed)				100 400	A A
$V_{SD} (*)$	Forward On Voltage	$I_{SD} = 100 \text{ A}$ $V_{GS} = 0$			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 100 \text{ A}$ $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 20 \text{ V}$ $T_j = 150^\circ\text{C}$ (see test circuit, Figure 5)		75 150 4		ns nC A

(*)Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

(•)Pulse width limited by safe operating area.

Safe Operating Area



Thermal Impedance

