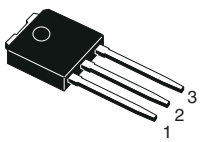
STD6NF10
STU6NF10

N-channel 100 V, 0.22 Ω, 6 A, DPAK, IPAK low gate charge STripFET™ Power MOSFET

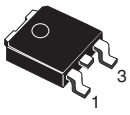
Features

Type	V_{DSS}	$R_{DS(on)}$ max	I_D
STD6NF10	100 V	< 0.250 Ω	6 A
STU6NF10	100 V	< 0.250 Ω	6 A

- Exceptional dv/dt capability
- 100% avalanche tested



IPAK



DPAK

Application

- Switching applications

Description

This Power MOSFET series realized with STMicroelectronics unique STripFET process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced high-efficiency, high-frequency isolated DC-DC converters for telecom and computer applications. It is also intended for any applications with low gate drive requirements.

Figure 1. Internal schematic diagram

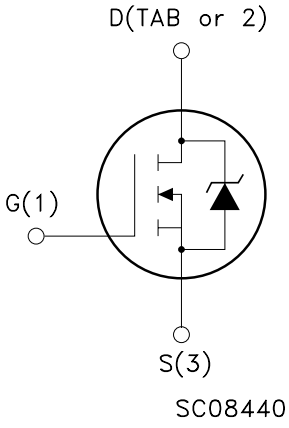


Table 1. Device summary

Order codes	Marking	Package	Packaging
STD6NF10T4	D6NF10	DPAK	Tape and reel
STU6NF10	6NF10	IPAK	Tube

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	100	V
V_{GS}	Gate- source voltage	± 20	V
I_D	Drain current (continuous) at T_C = 25 °C	6	A
I_D	Drain current (continuous) at T_C = 100 °C	4	A
I_{DM} (1)	Drain current (pulsed)	24	A
P_{tot}	Total dissipation at T_C = 25 °C	30	W
	Derating factor	0.2	W/°C
dv/dt (2)	Peak diode recovery voltage slope	40	V/ns
E_{AS} (3)	Single pulse avalanche energy	200	mJ
T_{stg}	Storage temperature	-65 to 175	°C
T_j	Max. operating junction temperature		

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 6$ A, di/dt ≤ 300 A/µs, $V_{DD} \leq V_{(BR)DSS}$, Tj $\leq T_{JMAX}$
3. Starting T_j = 25 °C, I_D = 3 A, V_{DD} = 50 V

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	5	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max	100	°C/W
T_J	Maximum lead temperature for soldering purpose	300	°C

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS} =0	100			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = max rating V_{DS} =max rating, T_C = 125 °C			1 10	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 3 A		0.22	0.25	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = > $I_{D(on)}$ x $R_{DS(on)max}$, I_D = 3A		34		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0		280 45 20		pF pF pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD} = 50 V, I_D = 3 A R_G = 4.7 Ω, V_{GS} = 10 V		6 10 20 3		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 80 V, I_D = 6 A, V_{GS} = 10 V, R_G = 4.7 Ω		10 2.5 4	14	nC nC nC

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%.

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)				6 24	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 6 A, V_{GS} = 0			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 6 A, di/dt = 100 A/µs, V_{DD} = 10 V, T_j = 150 °C		70 175 5		ns nC A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

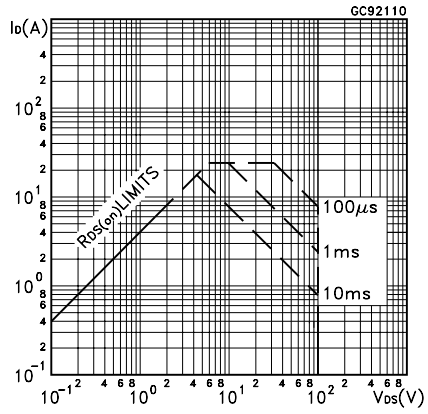


Figure 3. Thermal impedance

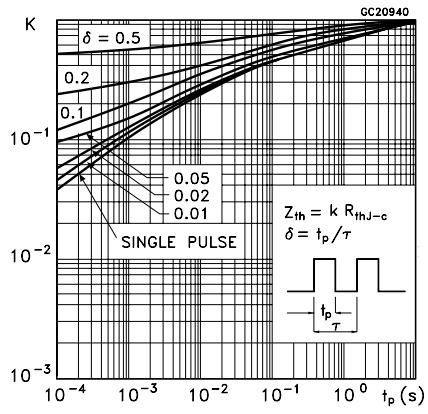


Figure 4. Output characteristics

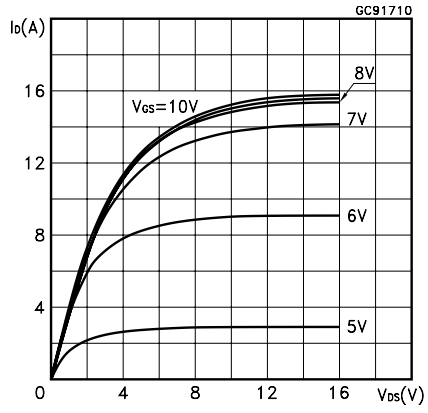


Figure 5. Transfer characteristics

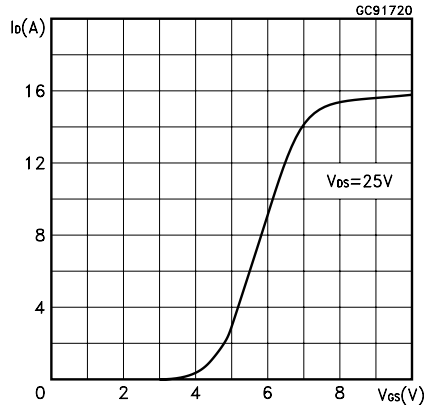


Figure 6. Transconductance

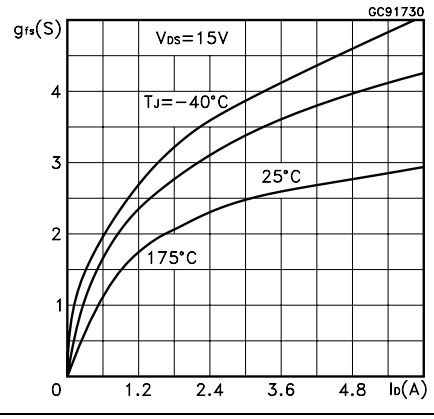
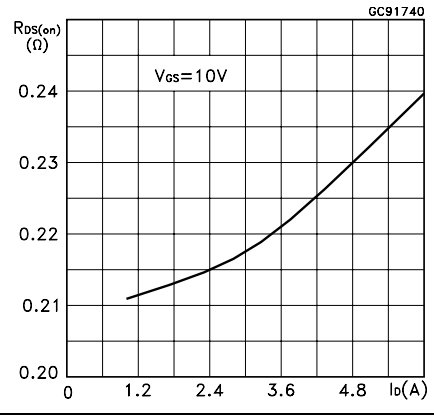



Figure 7. Static drain-source on resistance